# HYBRID MATERIALS AND PROCESSES FOR FLASH MEMORY GATE STACK

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# HYBRID MATERIALS AND PROCESSES FOR FLASH MEMORY GATE STACK

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Scaling conventional floating gate Flash memory faces extremely difficult challenges today. Novel structures in both the gate stack and channel have been adopted for better scalability while maintaining memory performance. Gate stack designs with discrete-charge storage such as nanocyrstal (NC) memory have demonstrated significant enhancement in retention to programming time ($t_R$ / $t_{PE}$) ratio at low program/erase (P/E) voltages and superior cycling lifetime. A 3D finite-element method (FEM) simulation was performed to assess the bit-error-rate (BER) due to the non-uniformity in NC size, position, and density distribution below the 30nm technology node.

To address the parametric variation for discrete-charge storage, hybrid approaches with integration of organic molecules, atomic-layer-deposited oxide, and solution-based processes offer better uniform charging capability by utilizing the bottom-up self-assembly method and the monodispersion nature of the molecules. We investigated barriers with thermally and electrically stable redox-active ferrocine (Fc) and cobalt-porphyrin (CoP) as well as alkyl-chain molecules in a well-studied metal-oxide-semiconductor (MOS) structure to better understand the charge storage, dielectric and interface properties of the molecular layers.

For charge storage, the density of CoP can be readily controlled to achieve three distinguishable memory states in a single cell at room-temperature. In addition, we employed CoP as a resonant tunneling barrier (RTB) that further extends the retention-to-program time ratio and cycling lifetime. Hybrid solution-based layer-by-

layer (LBL) deposition methods are demonstrated with various functional ends of the benzyl and alkyl molecules to create large area, electrically robust molecular junctions and insulation. Our approach provides a practical and promising way for the design and fabrication of silicon-based or all-organic nonvolatile memories.

## BIOGRAPHICAL SKETCH

Jonathan Shaw was born in Los Angeles, California, on October 2, 1982. He moved back to Hsinchu, Taiwan, at a young age and received education from elementary school to second year of high school. During his childhood, he knew his father was a brilliant student and very successful at work. The bar was set high, and he had to work extra hard to follow his footsteps. In 1998, he moved back to Irvine, California to finish high school and entered University of California, San Diego (UCSD) to study electrical engineering. During the final years of his undergraduate studies, he found his interest in device electronics and joined a summer research scholars program.

After finishing his undergraduate studies, he joined the MS/Ph.D. program at the school of Electrical and Computer Engineering, Cornell University in Ithaca, NY. His research interest focuses on the design and integration of hybrid organic/inorganic molecular-based memory.

To my parents, Ru-Wen Shaw and Li-Lian Chow

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CHAPTER 1

# INTRODUCTION

## *1.1 Emerging Memory Devices*

The demand for nonvolatile memory has outpaced the projection of Moore's law in logic integrated circuits for the past decade due to the fast growth of portable electronics and embedded device such as mobile phones, tablets, and solid-state drives [1]. NAND Flash memory, in particular, has aggressively dominated the memory market and remains one of the fastest growing segments in semiconductor industry. To date, the advance in NAND Flash technology has been mainly driven by geometric scaling. However, there are several show-stoppers related to CMOS scaling such as parasitic coupling, dielectric effects, and semiconductor transport [1-4]. First, as the density of memory cell is increased, nearby floating-gate (FG) coupling increases and poses disturbance to the memory state of neighboring cells. Second, the thickness of the tunnel oxide is limited by the stress-induced-leakage-current (SILC), which can lead to unacceptable charge retention and slow program/erase (P/E) operations. Muli-level-cell (MLC) has been developed to further improve areal density, but the resulting high P/E voltages will eventually offset the benefits due to larger power dissipation and poor endurance of the tunnel oxide after many P/E cycles. In addition, one needs to consider the inherent tradeoff associated with MLC to balance the programming accuracy and error correction capability with the space of necessary peripheral circuitry. In terms of device engineering, retrograde doping [7], FinFET [8], high-$\kappa$ dielectrics [9-12], and surround gate [13], are proposed to increase the channel coupling factor (CF) while limiting short channel effect (SCE). Strained SI was proposed to increase channel mobility and drive current [14-15]. Schottky source-drain (S-D) barrier and fully depleted silicon-on-insulator (SOI) lowers the S-D

resistances and improve transistor characteristics [16-17]. Discrete charge storage based devices such as silicon-oxide-nitride-oxide-silicon (SONOS) [18-27] and nanocrystal (NC) memories [28-46], provide isolated storage islands, which are immune to inter-node leakage. The discreteness also prevents significant charge loss due to localized percolation paths from SILC and enables further tunnel oxide scaling. These technologies can extend the lifetime of charge-based storage beyond the 45nm node. However, the fundamental threshold voltage ($V_{th}$) scaling is saturated by the 60mV/dec physical limit of the MOS structure and leakage power remains the bottleneck for advanced technology nodes. More importantly, the variation in $V_{th}$ of the P/E states must be tightly controlled and this remains a major drawback of the scaled NC memory cell as the fluctuation in the NC size and the NC number in each cell becomes substantial [47-49].

To address these issues, many alternative memory device structures have been under heavy research. Among the prototypical technologies are ferroelectric gate FET random access memory (FeFETRAM) [50], spin transfer torque magnetoresistive random access memory (STT-MRAM) [51], and phase-change random access memory (PRAM) [52]. For a single cell, all three technologies can outperform the current FLASH technology due to fast P/E and good reliability. However, replacing FLASH becomes a very challenging task for any emerging technologies to simultaneously achieve low-cost, high-speed, and high-density. FeFET suffers short retention due to destructive read and depolarization field and the scalability is limited by the thick Fe layer to achieve fast switching, and the programming voltage cannot be lowered due to required read/program disturb margin. Complicated film structures, process reliability concerns, and poor programming efficiency (write current > 100μA) limits the potential of large scale integration of STT-MRAM. PRAM, in particular, is projected to have the best scalability of all three, but lowering the reset current (≥

40μA) remains to be a major concern for cost-effective manufacturing [53]. This is very challenging considering the limited current drive capacity of scaled access transistors. In addition, all structures suffer either parasitic or thermal coupling with adjacent cells. More importantly, thorough research at the integration level will be required since the device structure and operation principle are very different from conventional FLASH cell.

Meanwhile, molecular memories have had negligible impact in electronic circuits because the charging physics is often not well understood. Integration is further hindered by the low thermal budget and difficulty in forming a stable electrode contact. However, as the processing cost increases with each technology node, molecular memories offer several distinct advantages. Large area production and cheap processing methods such as spin-coating [54], ink-jet printing [55] or solution based self-assembly process [57-60] have been demonstrated on plastic, glass, or inorganic substrates. Also, the molecular properties can be tailored with the choice of chemistry and geometry for possible layer-by-layer integration, improved compatibility with existing CMOS technology, and application in bio-sensor application.

## *1.2 Molecular Memory*

To understand electron transport and storage properties of molecular memory, it is useful to briefly review the concepts of molecular orbital (MO) theory and Coulomb blockade effect in a tunnel junction.

### 1.2.1. Molecular Orbital (MO) Theory

Electrons with a fixed energy have a fixed spatial distribution called an orbital. The electron spatial and energy can be predicted by calculating the Schrödinger

equation. Assuming only orbitals with approximately the same energy interact to a significant degree, molecular orbitals (MO) are formed when atomic orbitals (AO) overlap to form a bonding molecular orbital and an anti-bonding molecular orbital. The bonding molecular orbital results from an in-phase interaction, leading to an increase in the electron density between the nuclei. The greater plus-minus field attraction between the nuclei results in a more stable state and lower potential energy. Anti-bonding MOs are formed when the electrons interact out of phase and remain stable in separate AOs. The decrease in plus-minus electric field between the nuclei leads to a higher potential energy state.

Depending on the overlap orientations of the MOs, bonds are separated into two categories, as illustrated in Figure 1-1. End-on interaction results in σ MOs that are symmetric about the bond axis. Side-to-side overlap results in $\pi$ MOs that are asymmetrical about the bond axis. The interaction is usually stronger for σ bonds compared to $\pi$ bonds. As a result, the $\pi$ orbitals usually lie between the bonding and anti-bonding σ orbitals. Similar to the concept of energy bandgap, the energy separation between the Lowest Unoccupied Molecular Orbital (LUMO) and the Highest Occupied Molecular Orbital (HOMO) is defined as the HOMO-LUMO gap. The combined knowledge of the HOMO-LUMO gap and how these energies align with the surrounding metal or insulator materials are key considerations in understanding molecular transport.

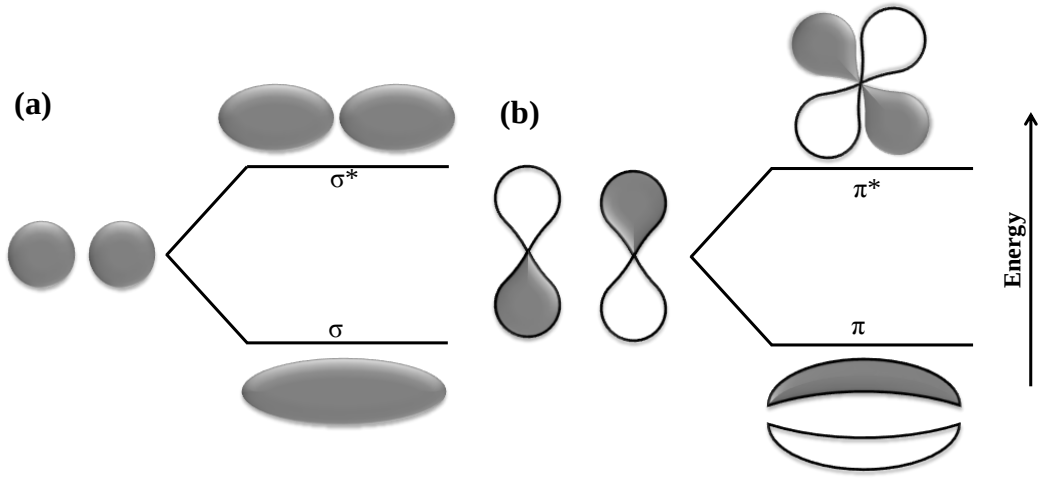



Figure 1-1 Two overlapping *s* orbitals or *p* orbitals forming (a) σ and (b) $\pi$ bonds, respectively.

A conjugated system is formed when multiple p-orbitals electrons are delocalized in vast compounds with alternating single and double bonds. In most cases, the overall energy of the molecule is lowered and the stability is increased. Aromatic compounds such as benzene are of particular interest due to its unusual stability from enhanced electronic coupling. The associated high thermal budget and chemical inertness is attractive for applications in molecular electronics. In addition, stronger electron coupling in highly conjugated systems such as porphyrin results in smaller HOMO-LUMO energy gap, which enhances the electron conductivity significantly.

### 1.2.2. Coulomb Blockade Effect

To understand the operation principle of electrons tunneling across a thin insulating barrier into a small volume that is in the nanometer regime, the Coulomb blockade effect is briefly reviewed here. The tunnel junction capacitor is charged with the first tunneling electron if the chemical potential of the storage node is lower than the electrode. For additional electron storage, the energy that is needed to overcome

the Coulomb repulsion energy is called the single-electron charging energy. As illustrated in Figure 1-2, the total energy that is required, $\Delta E$, is the charging energy plus the energy separation resulting from the quantum confinement effect.

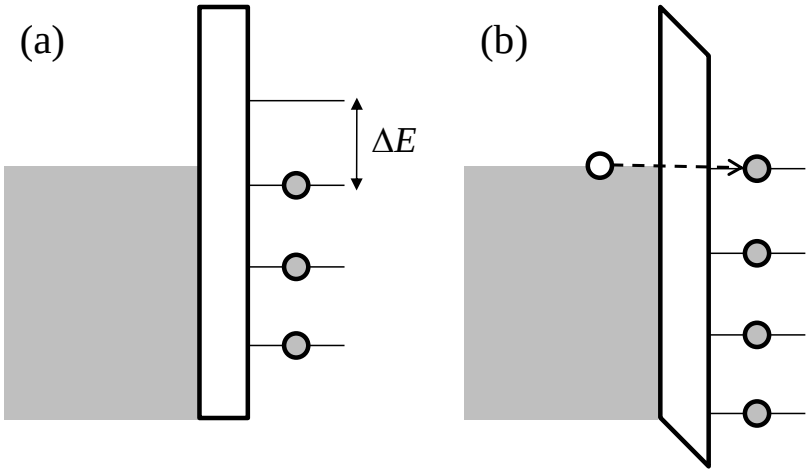



Figure 1-2 Energy band diagram of electrons tunneling from the electrode into the energy levels of the storage dot. In (a), electrons are blocked by the combined Coulomb blockade and quantum confinement energies. In (b), electron transport probability is increased as the electrode Fermi energy approaches the energy levels of the dot.

The charging energy is $e^2 / C$, where $e$ is the elementary charge and $C$ is the self-capacitance of the storage node. To the first order approximation, the self-capacitance is proportional to the size of the storage node. Coulomb blockade is most commonly observed in single electron transistor device [61], consisting a nandot sandwiched between two tunnel junctions. The potential of the island can be tuned by the third gate electrode by capacitive coupling. In Figure 1-2 (a), the electrons have no accessible states to tunnel through. When the potential of the gate electrode is increased so that the island potential is lower than the electrode by the total charging energy (Figure 1-2 (b)), electrons can tunnel into the island and the conductance increases. In order to observe Coulomb blockade, two conditions must be satisfied, assuming ideal contact electrodes. First, the temperature must be low enough so that

the thermal energy is much lower than the total charging energy and electron tunneling by thermal excitation is inhibited. Second, the tunneling resistance must be greater than the resistance of a quantum point contact, $h / e^2$, derived from the Heisenberg's Uncertainty principle. For demonstration purposes, we will integrate redox-active molecules in a simple MOS structure to observe the Coulomb staircase associated with the charging energy in Chapter 3.

### 1.2.3. Molecular Memory Devices

Although organic electronics have attracted intensive research in recent years, performance optimization is often hindered by the lack of distinction of the compounded effects from inorganic semiconductors/dielectrics and their interfaces. Molecular memory states are usually sensed in two ways: one based on resistivity change and the other on capacitance charging. For resistive change molecular memories, a critical field is usually necessary to change the conformation of the molecule. The conformation change often leads to a change in barrier height and conductance. One example is the electrically driven molecular rotor device [62], which demonstrates a bi-stable resistivity switch with an on/off ratio of approximately $10^4$, a read window of about 2.5V, and retention up to $10^4$ s. However, the resistivity based molecular memories usually involve some complications due to its metal-molecule-metal structure. Not only is it difficult to deposit a stable top electrode, the state of the molecules are also prone to interactions with the metal electrodes or metal migration. A strong coupling between the electrode and the molecule may lead to molecule-independent switching and modification of the intrinsic spacing of the energy levels, which makes it difficult to study the molecule-specific behaviors.

Compared to resistivity based structure, capacitance charging may be a more viable approach. A hybrid Si-molecular structure has been proposed by Misra *et al*

[57-59]. Redox-active molecules are self-assembled on either a Si or $SiO_2$ substrate and the potential of the molecules can be set by the surrounding electrolyte, which is tunable by the gate electrode. Cyclic-voltammogram (CyV) is the main technique for sensing the change in conductance associated with the charging and the discharging of the carriers stored at the MOs.

Alternatively, we propose a hybrid organic-inorganic dielectric structure in a well-understood metal-oxide-semiconductor (MOS) structure with low process temperature to first study the electrical insulation and charge storage properties in various molecular choices [60]. The MOS-based structure is more attractive for several reasons. In contrast to the low-impedance connection used CyV, one creates a high-impedance nonamperometric electrode on either side of the molecule to probe the molecular redox states, which further lessen the possibility of orbital hybridization from the gate. In addition, the lack of an insulating layer will significantly limit the charge retention time. Furthermore, the operation speed is enhanced significantly with an all-electron conduction mechanism in the proposed structure. More importantly, the proposed structure has a standard Flash memory gate stack and is CMOS compatible. The mono-dispersion nature of the molecules combined with the freedom to control the density of the redox-active molecules with dummy molecules enable precise-step charging to the MOs. This can potentially pave the way for building a multi-bit single cell without the need of complicated peripheral circuits that is usually necessary to control the MLC operation of FLASH memory.

A detail report on the integration and memory characteristics of various molecules in a standard Flash memory gate stack will be discussed in Chapter 3.

### 1.2.4. Molecular Tunnel Barrier

For memory devices in general, the tunnel barrier needs to provide field-sensitive carrier transport so that the charge injection and removal can be very fast in high electric fields while charge retention can be very long at low electric fields. Field-sensitive barrier engineering is a well studied method to enhance the retention time ($t_R$) to programming time ($t_{PE}$) ratio of memory devices [21], [23], [63-66]. For example, a composite tunnel barrier of a thin $SiO_2$ and a thick $HfO_2$ with a relatively smaller bandgap and higher dielectric constant utilizes the field asymmetry during P/E and retention operation. As illustrated in Figure 1-3, during programming, electrons can readily tunnel through the composite barrier due to the much stronger field dependence of the $HfO_2$ layer by Fowler-Nordheim (FN) tunneling. At low electric fields, direct tunneling (DT) through the thick composite barrier is the only conduction mechanism, resulting in small transmission probability back to the substrate or superior retention.

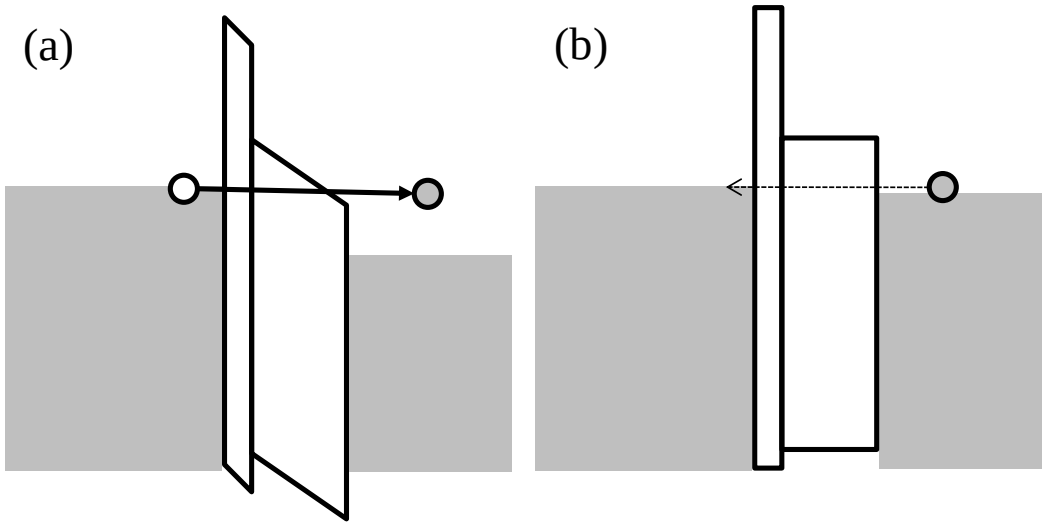



Figure 1-3 Energy band diagram representations during (a) program and (b) retention conditions with a thin $SiO_2$ and a thick $HfO_2$ barrier.

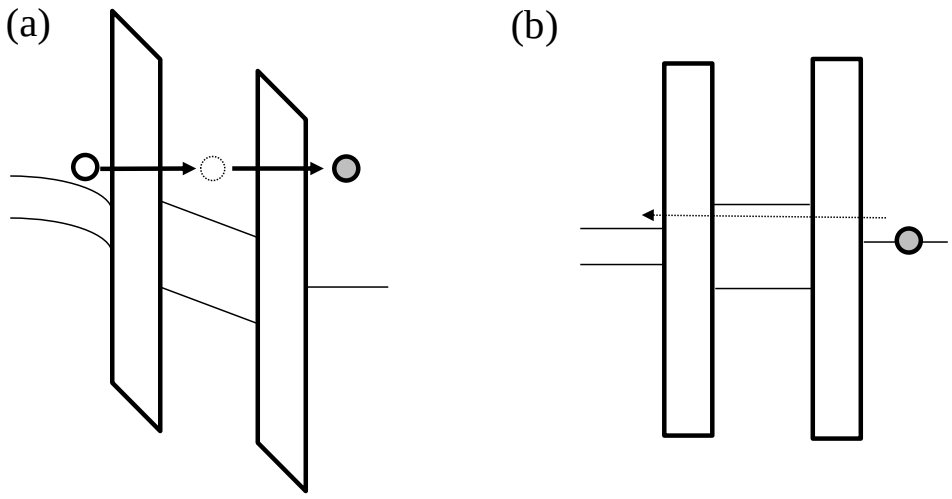


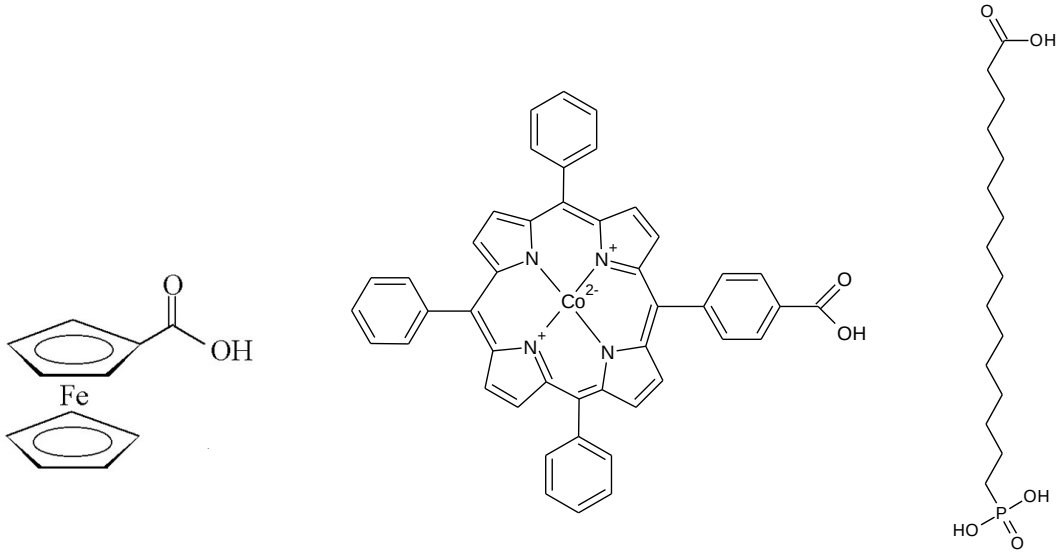

Figure 1-4 Energy band diagram representations of a double tunnel junction during (a) programming and (b) retention conditions.

Following similar principles, redox molecules with small HOMO-LUMO gap can be embedded in between two large bandgap dielectric layers to form a resonant tunneling structure, as illustrated in Figure 1-4. At high electric field, the MOs provide intermediate states for resonant tunneling, and significantly enhance the carrier transmission probability. At retention or low field operation, carrier transmission probability is suppressed by the HOMO-LUMO gap and charging energy. The field asymmetry gives rise to superior $t_R$ / $t_{PE}$ ratio [43]. We will illustrate an example with redox-active cobalt porphyrin molecules acting as the resonant tunneling node in a NC memory structure in Chapter 4.

## *1.3 Molecule Selection*

Typically, the molecule can be separated into three components: a charge storage medium, a head group to form a self-assembled monolayer (SAM) with the underlying substrate, and a tail group that can be utilized for layer-by-layer integration. Specific to this study, either carboxylic acid (COOH) or phosphonic acid

(PA) head groups are used to form densely packed SAM on $Al_2O_3$ or form amide bonds with amine groups. COOH can also be added as a tail group to covalently bond with the trimethyl aluminum (TMA) precursor of atomic-layer-deposition (ALD) of




(a) (b) (c)

Figure 1-5 Molecular schematics of (a) Ferrocene functionalized with COOH (FcCOOH), (b) Cobalt-porphyrin (CoP), and (c) functionalized alkane chain (PHDA).

$Al_2O_3$ [67-69]. Stable chemical bonding results in defect free interface, which may alleviate SILC and provide superior cycling endurance.

Our memory structure includes three main classes of molecules: redox-active molecules such as ferrocene (Fc), cobalt-porphyrin (CoP) and functionalized alkane chains such as hexadecanoic acid (PHDA). The molecular schematic is illustrated in Figure 1-5.

Fc is an organometallic compound with two cyclopentadienyl rings bound on opposite sides of the central iron. Porphyrins are aromatic compounds that are composed of four interconnected modified pyrrole subunits. Porphyrins can readily

bind with metals to form metalloporphyrins such as CoP. Fc has one reversible redox state and CoP usually exhibits two to three reversible redox states. The stable orbital states can potentially be used as multi-bit electron storage in a single cell. Fc and CoP have decomposition temperature of approximately 250°C [70] and 400°C [71], respectively. From the perspective of manufacturing, a high thermal budget is usually required for standard CMOS processing. To control the inter-distance between the redox-active molecules, dummy molecules with similar molecular structure but without any redox states are usually mixed with the redox-active molecules to suppress neighbor Coulomb repulsive field, which can fluctuate the charging energy and inhibit uniform step-charging.

Alkane chains are simple chemical compounds that consist of only hydrogen and carbon atoms bonded by single bonds, and each carbon atom has 4 C-H or C-C bonds. A functionalized alkane can self-assemble on the desired substrate and form a densely-packed monolayer, which exhibits attractive properties for molecular electronics application [72-74]. For example, alkane chain with a silane terminal group such as octadecyltrichlorosilane (OTS) (the chain length can be varied from 0.8 to 2.8 nm) has demonstrated excellent insulating characteristics, with leakage current densities in the order of $10^{-8}$ A $cm^{-2}$ at an average field of 5.8 MV/cm and a breakdown field of 12 MV/cm [72]. In addition, the OTS monolayer is thermally stable up to 450°C. The relatively high thermal budget allows forming gas-annealing, which reduces the interface state density from $10^{12}$ to $10^{11}$ $cm^{-2}$ $eV^{-1}$, which is comparable to that of the $Si/SiO_2$ interface.

The densely packed SAM can thus be considered as the tunneling dielectric in a conventional MOS structure. For this study, our goal is to form a SAM with either a phosphonic or carboxyl head group on metal oxide, which has been demonstrated in

previous literatures [73-74]. We will further study the insulating properties of PHDA, a modified alkyl chain, in a resonant tunneling structure in Chapter 4.

## *1.4 Chapter Organization*

This dissertation intends to study the charge behaviors of a hybrid organic/inorganic molecular memory structure in great detail. A thorough understanding of the storage, insulation and interface properties of organic dielectrics in a conventional MOS structure will pave the way for the design and fabrication of all-organic substrates, which offer an even broader range of applications in large-area energy, displays and sensors.

Chapter 2 presents a 3-D fininte element analysis on the BER of metal NC memories with variation in size, density, and location for aggressively scaled device. The BER study will be performed on both bulk and nanowire (NW) substrates to further examine the fringing field effect on NC to substrate coupling and how it influences the threshold voltage variation.

Chapters 3 and 4 are the main body of this thesis. In Chapter 3, we will introduce the integration method of redox-active molecules in a MOS structure and demonstrate the multibit storage capability at room temperature. CoP molecules will be further employed as a resonant tunnel barrier with the possibility of simple solution based layer-by-layer integration in Chapter 4.

Chapter 5 discusses the Boron (B) diffusion effect at the CoFeB/MgO interface through electrically characterization. Recent studies have shown extremely high TMR with a sputtered CoFeB/MgO/CoFeB magnetic tunnel junction (MTJ). It is believed that B diffuses into MgO via vacancies to form Mg-B-O after annealing, which exhibits a sharper interface, improving spin-filtered coherent tunneling and high TMR. CoFeB/MgO/Si MOS capacitor structures were made to independently estimate the

interface traps and determine its correlation with the TMR ratio and associated reliability.

Finally, Chapter 6 concludes the dissertation with suggestion for future work.

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CHAPTER 2

# STATISTICAL METROLOGY OF METAL NANOCRYSTAL MEMORIES WITH 3D FINITE-ELEMENT ANALYSIS

## *2.1 Abstract*

We study the parametrical yield of memory windows for the metal nanocrystal (NC) flash memories with consideration of the 3D electrostatics and channel percolation effects. Monte Carlo parametrical variation that accounts for number and size fluctuations in NCs as well as channel length is used to determine the threshold voltage distribution and bit error rate (BER) for gate length scaling to 20 nm. Devices with nanowire-based channels are compared with planar devices having the same gate stack structure. Scalability prediction by 1D analysis is found to be very different from 3D modeling due to underestimation of effective NC coverage and failure to consider the 3D nature of the channel percolation effect.

## *2.2 Introduction*

Due to the scaling limit of gate length and tunneling oxide thickness, it is difficult for conventional floating gate memories to achieve required retention and interference characteristics while maintaining low-voltage program/erase (P/E) operations [1]. To overcome this inherent design limitation, nanocrystal (NC) [2] memory is considered as one of the promising candidates that enable reduced inter-cell floating gate coupling, tolerance to local dielectric defect, low P/E voltage, fast P/E speed, and compatibility with current CMOS technology [3-7]. In particular, metal NC memories can potentially push further scaling due to large density of states, inherent field enhancement, selectable work function and tunneling asymmetry between P/E and retention [5, 7]. Furthermore, Coulomb blockade energy can be

reduced by replacing the insulating layer in the gate stack by high-κ dielectric, which also leads to an increasing in channel-NC coupling due to the field enhancement effect [6, 8].

Fluctuation in memory window due to NC size/density/registry variations and gate length is one of the main concerns for scalability [9, 10]. The goal of this paper is to illustrate the importance of the 3D electrostatics and channel percolation effects that are not considered in previous Monte-Carlo (MC) statistical metrology of NC memories [9-15]. The new model can be used for more accurate scaling prediction. We perform the MC parametrical analysis, with inner loops by the finite-element (FE) solver in COMSOL$^{TM}$, to predict the threshold voltage ($V_{th}$) variations and corresponding bit error rate (BER). Furthermore, nanowire (NW)-based memories with sub-10 nm Si-channel width have been proposed to obtain large $V_{th}$ shift and longer charge-retention by the bottleneck and quantum confinement effects [16]. Metal NC memory with nanowire (NW) [17] channel is studied in comparison with the planar device for $\Delta V_{th}$ variation analysis. Simulation results indicate that the high percentage of erratic bits will still be one of the main concerns for NW devices with sub-30 nm gate length due to NC number density variation. Previously, it has been shown that preferential self-alignment (SA) of NC to the carbon nanotube (CNT) can be achieved [18]. Preferential growth of NC near the channel can offer an effective solution to NC density variation.

## *2.3 Device Modeling and Assumptions*

Schematics and a sample mesh of the simulated planar and NW devices [17] are shown in Figure 2-1 and Figure 2-2, respectively. Our model assumes a p-type silicon substrate with $10^{17}$ cm$^{-3}$ doping. For planar devices, a halo-doping profile is

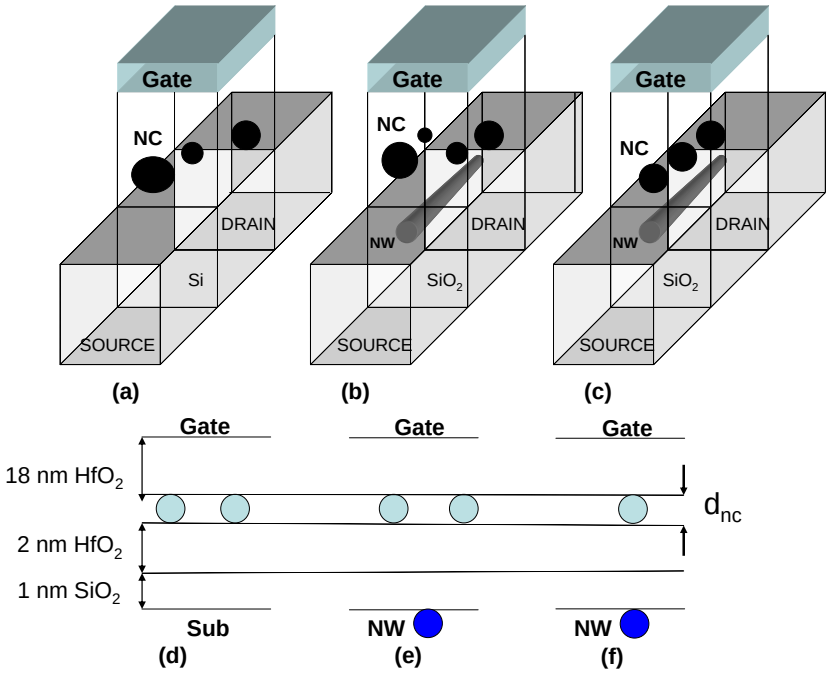



Figure 2-1 Schematic of metal NC flash memory with (a) a planar channel, (b) a nanowire channel and (c) a nanowire channel with self-aligned (SA) NCs. For the SA case, each NC is centered at locations on top of the channel region. The corresponding cross-section views are shown in (d), (e), and (f), respectively. Simulation parameters of the structure: NC diameter $d_{nc}$: 6.1 nm; NW diameter: 3 nm; average NC density: $5.0 \times 10^{11}$ $cm^{-2}$; tunneling oxide: 2 nm $HfO_2$ on top of 1 nm $SiO_2$; control oxide: 18 nm $HfO_2$.

added to control short channel effects (SCE) and the channel width is fixed at 20 nm. Spherical NCs are embedded in a gate stack with 18 nm $HfO_2$ control oxide and a heterogeneous tunnel dielectric of 2 nm $HfO_2$ and 1 nm $SiO_2$ [8]. The NC diameter is 6.1±1.2 nm and the average number density is $5.0 \times 10^{11}$ $cm^{-2}$ with percentage fluctuation of 51% and 34% for 20 and 30 nm channel lengths, respectively, following the experimental distribution from unconstrained self assembly in a gate-first process [19]. Gaussian variations of NC size and channel length, Poisson variations of NC

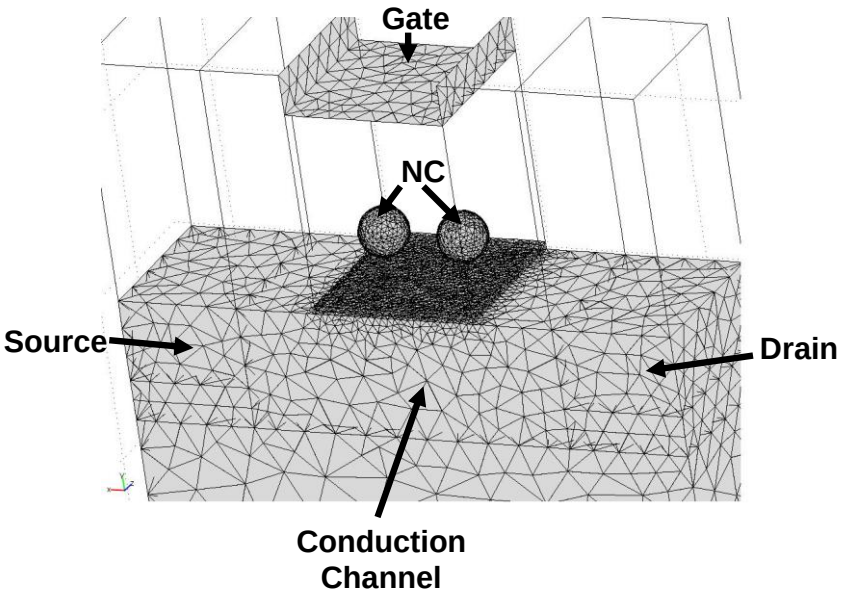



Figure 2-2 Sample mesh of the planar device with 20 nm gate length in the COMSOL™ finite-element solver.

number density, and uniform variation on NC registry have been included in the MC simulation, with statistics extracted from the experiments [17-20]. The NW device is 3 nm in diameter [17] and has the same gate stack structure, doping level (but without halo), and source/drain structures as the planar device for direct comparison. All simulation cases assume an electrostatic environment, where the NCs either remain charged with five electrons or uncharged, for calculating the control gate characteristics, unless stated otherwise. Our finite-element model consists of 3D Poisson and modified drift-diffusion formalisms, implemented by COMSOL [21]. It does not include detailed quantum transport effects that can enhance the accuracy for sub-90 nm above-$V_{th}$ currents [22]. We also ignore quantum confinement and band-splitting effects, which may be important in NW devices [23-24]. The classical transport is used to maintain acceptable computational efficiency in the statistical metrology of 3D geometrical design, where total computation can be accomplished in several weeks on a 64-bit CPU, 8 GB memory platform. For $\Delta V_{th}$ fluctuation

prediction, our simulation model should be acceptable since 3D electrostatics and channel percolation below $V_{th}$ are self-consistently considered. We define BER as the probability of a programmed bit with an offset in $V_{th}$ that falls below the nominal '0' state plus a fixed voltage $V_{tol}$, which is determined by the sense amplifier tolerance. Table I shows the simulated Gaussian fitted mean threshold voltage shift, $\mu(\Delta V_{th})$, and standard deviation, $\sigma(\Delta V_{th})$, for various device structures.

## *2.4 Results and Discussion*

### 2.4.1. The Fringing-Field Effect and Comparison with 1D Analytical Model

To have a qualitative understanding on $V_{th}$ fluctuation to account for 3D electrostatics, we can describe the nominal memory window $\Delta V_{th}$ in a semi-empirical model as [9, 20]:

$$\Delta V_{th} = R \cdot \frac{e \cdot N}{C} \tag{1}$$

where $e$ is the elemental charge, $R$ is a constant representing the relative strength of channel-NC coupling, $C$ is the 3D NC-to-control-gate coupling capacitance, and $N$ is the number of electrons stored in each NC. The nominal memory window $\Delta V_{th}$ as well as $V_{th}$ fluctuations increases with increasing $R$ through effective NC coverage over the channel. Clearly, the charge in a NC perturbs the channel potential on a larger coverage area than the NC cross sectional area due to the fringing effect [20]. As shown in Figure 2-3, $\Delta V_{th}$ estimated by the 3D MC FE solver is significantly greater than the cases where the coverage area is assumed to be the NC cross-sectional area in semi-1D models. Good agreement can be obtained between the 3D model [20] and the MC FE solver for $\Delta V_{th}$ versus the number charges stored in each NC. Due to the discrete nature of NC array and the spherical shape of NC, $\Delta V_{th}$ and $V_{th}$ fluctuation prediction must be calculated rigorously considering the entire 3D potential profile in the channel.

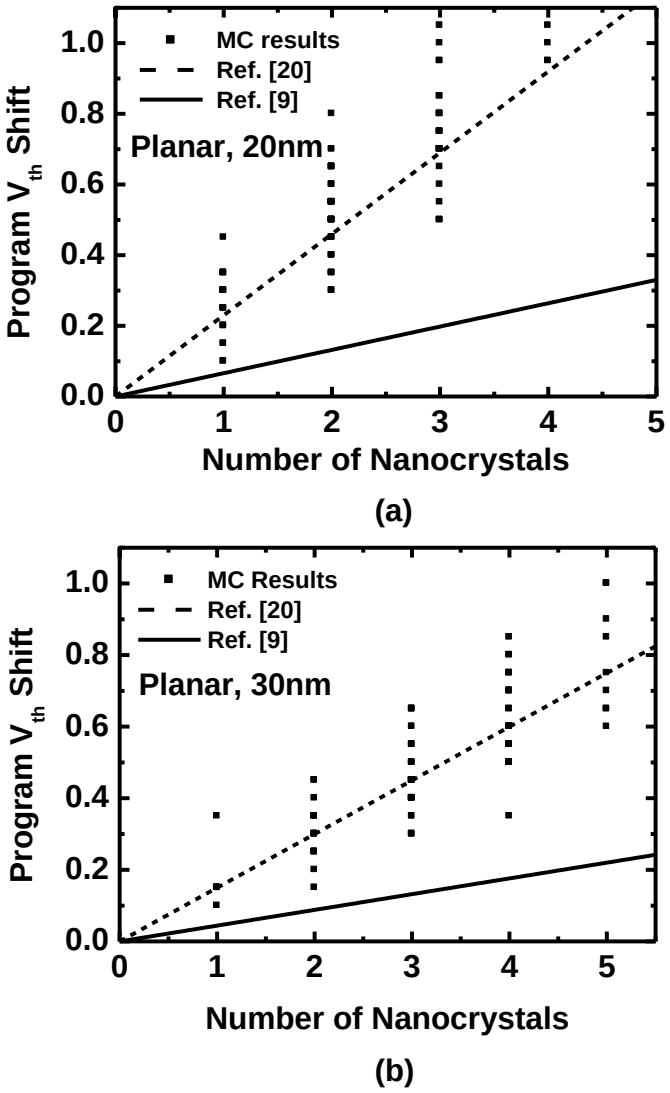



Figure 2-3 Threshold voltage shift after programming versus the number of NCs within each planar device with (a) 20 nm and (b) 30 nm gate lengths. Five electrons are stored in each NC. Semi-1D analytical model assumes that the coverage area is equal to the NC's cross-sectional area, whereas 3D model incorporates the fringing field enhancement effect on channel-NC coupling. 100 cases were simulated for each scenario.

Figure 2-4 shows the potential contours of a NW device with NC located directly on top and away from the channel, where the channel potentials are affected by the NC fringing fields and the corresponding I-V curves for NW devices with 3 nm and 7 nm diameters.

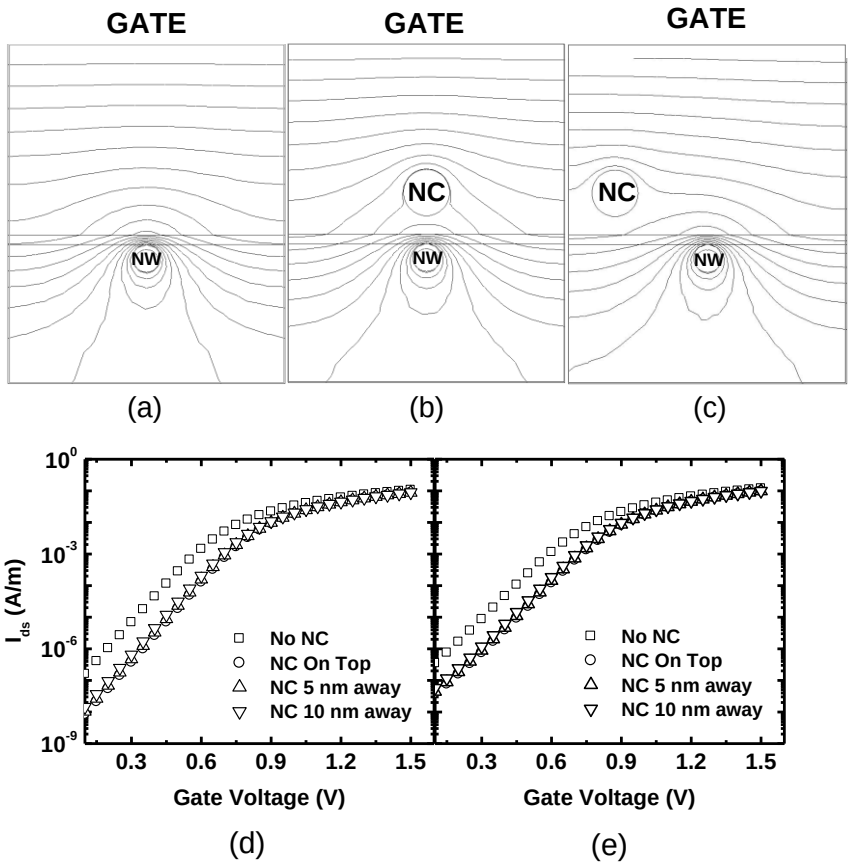



Figure 2-4 Cross-sectional view of the 3D electrostatic potential contours of the nanowire devices with (a) no NC, (b) one NC centered on top of the nanowire and (c) one NC centered10 nm away from the nanowire. Five electrons are stored in each NC. $V_G$ = 2 V and the contour spacing is 90 mV. Also shown are the corresponding I-V curves of (d) 3 nm and (e) 7 nm-diameter nanowire devices with no NC, one NC centered directly on top of the nanowire, and one NC centered either 5 nm or 10nm away from the nanowire.

We have found minute fluctuation in $\Delta V_{th}$ from NC registry variation in planar or NW devices, which suggests an enhanced channel-NC coupling dominated by the fringing field effect. However, the NC registry can affect the charging state during the P/E operations in the NW device since the tunneling length and hence the program current can be very different. We consider two asymptotic scenarios: full coverage (FC), where every NC in the gate stack is uniformly charged, and partial coverage (PC), where only NCs overlapping the NW channel are charged. Figure 2-5 compares $\Delta V_{th}$ distribution plots for the PC and FC configurations. The design combination of planar and NW devices is summarized in Table 2-1. Due to the fringing fields coming from NCs that do not overlap with the NW, devices A and D show larger $\Delta V_{th}$ and slightly tighter distribution than devices G and I.

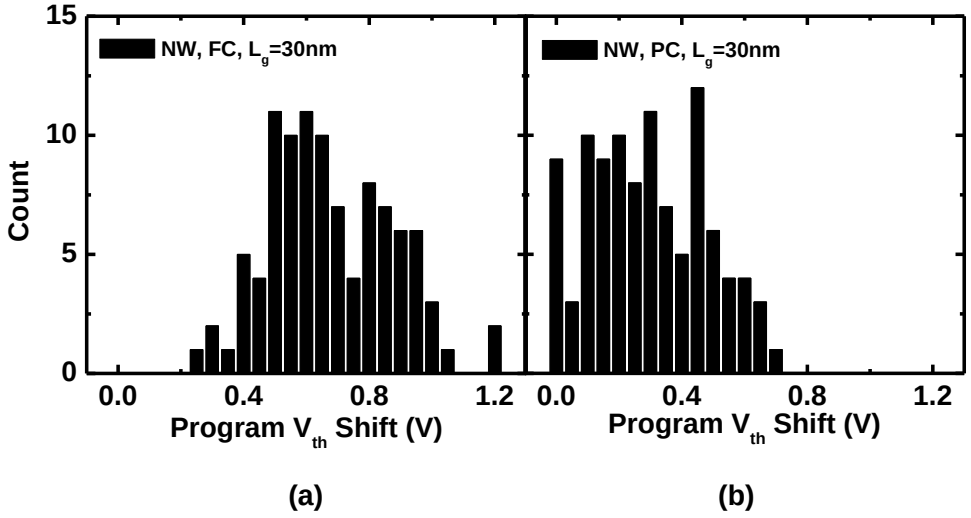



Figure 2-5 Monte Carlo simulation results showing the $\Delta V_{th}$ distribution of the scenarios where (a) all the NCs within the gate area are charged (FC), or (b) only the NCs that overlap with the channel region are charged (PC). The nanowire is 3 nm in diameter and 30 nm in gate length. Five electrons are stored in each NC. 100 cases were simulated for each scenario.

| Device | Channel Type | Gate Length (nm) | Diameter/ Width (nm) | $\mu(\Delta Vth)$ (V) | $\sigma(\Delta Vth)$ (V) | BER $V_{tol}$ = 0.1 V |
|---|---|---|---|---|---|---|
| A | Planar | 20 | 20 | 0.50 | 0.27 | $3.85 \times 10^{-2}$ |
| B | Planar | 30 | 20 | 0.47 | 0.19 | $1.92 \times 10^{-2}$ |
| C | Nanowire, FC | 20 | 3 | 0.53 | 0.28 | $3.41 \times 10^{-2}$ |
| D | Nanowire, FC | 20 | 7 | 0.41 | 0.26 | $6.65 \times 10^{-2}$ |
| E | Nanowire, FC | 30 | 3 | 0.65 | 0.21 | $3.4 \times 10^{-3}$ |
| F | Nanowire, FC | 30 | 7 | 0.53 | 0.23 | $3.15 \times 10^{-2}$ |
| G | Nanowire, PC | 20 | 3 | 0.16 | 0.29 | $1.87 \times 10^{-1}$ |
| H | Nanowire, PC | 20 | 7 | 0.17 | 0.33 | $1.64 \times 10^{-1}$ |
| I | Nanowire, PC | 30 | 3 | 0.24 | 0.26 | $1.42 \times 10^{-1}$ |
| J | Nanowire, PC | 30 | 7 | 0.34 | 0.21 | $7.54 \times 10^{-2}$ |
| K | Nanowire, SA | 20 | 3 | 0.32 | 0.11 | $2.27 \times 10^{-2}$ |
| L | Nanowire, SA | 30 | 3 | 0.53 | 0.10 | $1.52 \times 10^{-6}$ |

Table 2-1 Gaussian fitted mean threshold voltage shift, $\mu(\Delta V_{th})$, standard deviation, $\sigma(\Delta V_{th})$, and bit error rate with $V_{tol}$ = 0.1 V. Full coverage (FC) cases refer to the cases where all NCs have five electrons stored. Partial coverage (PC) cases refer to the cases where only NCs centered on top of the channel region are charged. Self-aligned (SA) cases refer to the cases where the NCs are self-aligned on the carbon nanotube by surface energy preference.

In either the 1D [9] or 3D [20] analytical models, the mean threshold voltage shift, $\mu(\Delta V_{th})$, and the standard deviation, $\sigma(\Delta V_{th})$, can be approximated by

$$\mu(\Delta V_{th}) = R \cdot \frac{e \cdot N}{C} \cdot \overline{N_{td}} \tag{2}$$

$$\sigma(\Delta V_{th}) = \mu\Delta V_{\text{th}} \cdot \sqrt{\frac{\sigma^2 N_{td}}{\overline{N_{td}}^2} + \frac{1}{\overline{N_{td}}} \cdot \frac{(\sigma(R))^2}{\overline{R^2}^2}} \tag{3}$$

where $\overline{N_{td}}$ is the average number of NCs and $\sigma(R)$ is the standard deviation of substrate-NC coupling factor. Fig. 6 compares $\mu(\Delta V_{th})$, $\sigma(\Delta V_{th})$ and BER as a function of gate length for the analytical models by Eqs. (2) and (3) [9, 20] and Gaussian-fitted MC simulation. It has been shown that $R$ is a relative weak function of NC diameter

when the channel coupling is adequate [20]. Since Gaussian-fitted parameters agree well with the 3D analytical model, the variation in $\Delta V_{th}$ is mainly determined by density fluctuation according to Eq. (3). However, previous semi-1D models [9-15] excluding 3D fringing and channel percolation underestimated NC coverage, resulting in severe parametric distribution distortion.

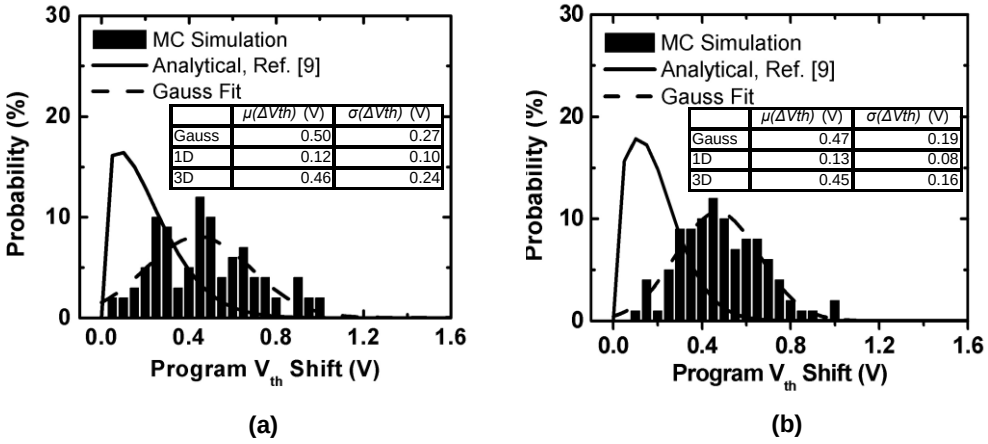
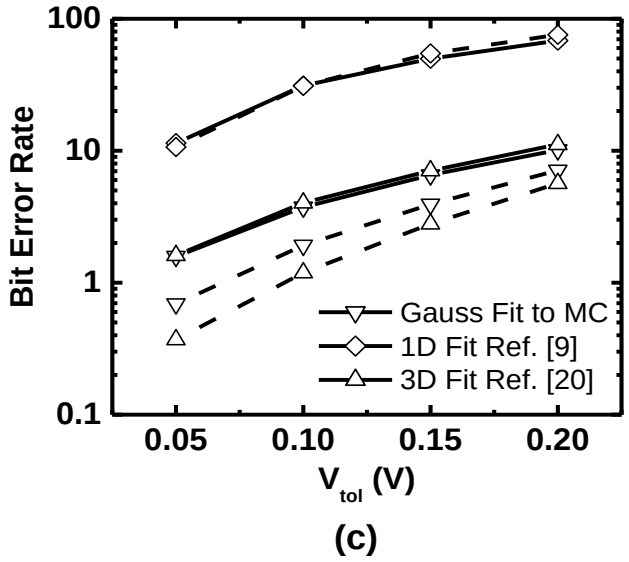



Figure 2-6 $\Delta V_{th}$ distribution probability density curves for planar devices with (a) 20 nm and (b) 30 nm gate lengths. Gaussian-fitted and semi-1D analytical models are also shown. The inset is a table comparing μ($\Delta V_{th}$) and σ($\Delta V_{th}$) estimated by semi-1D, full 3-D electrostatic, and Gaussian-fitted models. Plot (c) compares the corresponding bit error rates (BER) calculated from the three models versus $V_{tol}$. The solid lines represent the 20 nm device and the dashed lines represent the 30 nm device.




### 2.4.2. Impact of Gate Length and Nanowire Diameter

The channel percolation effect of the planar structure is illustrated in Figure 2-7. Typically, the percolation effect is enhanced with increasing channel *W/L* ratio, resulting in more severe $\Delta V_{th}$ fluctuations [11]. Figure 2-8 shows the percentage increase in BER for various device structures by scaling down the effective gate length from 30 nm to 20 nm. For gate length scaling with fixed channel width, the number of percolation paths available increases and higher BER is observed. As the diameter of NCs becomes larger than the diameter of NW devices, channel-NC coupling is enhanced and the number of percolation path vanishes in comparison with planar devices. Devices with larger NW diameter (B and E) have larger BER than the smaller ones (A and D) in FC charging as shown in Table 2-1, dominated by the fringing field effect. In contrast, devices I and J with PC charging show a decreasing BER with increasing NW diameter due to $\Delta V_{th}$ sensitivity to NC density variation when NCs away from channel is not charged and do not exert additional fringing fields.

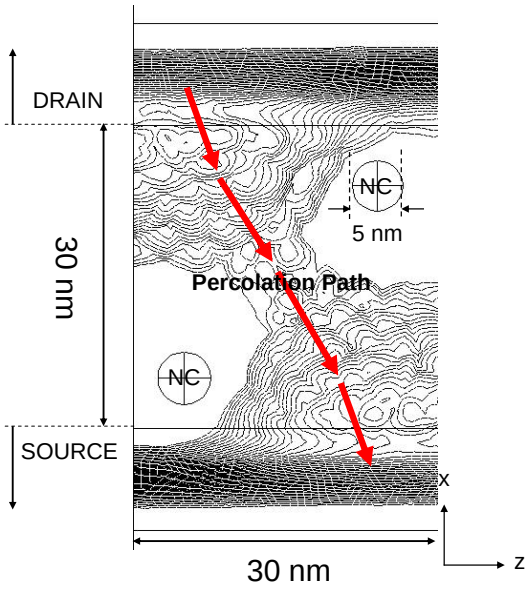



Figure 2-7 The contour plot of electron density for a 30 × 30 nm planar device. Each NC is charged with one electron. Electrons in the channel are screened by the NC and the dominant percolation path of the channel leakage current is highlighted.

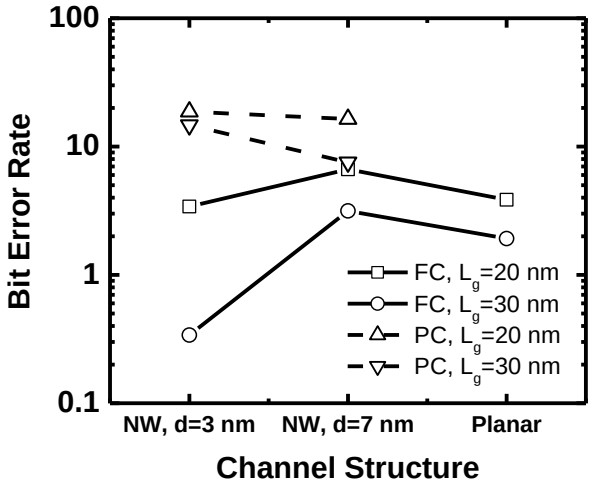



Figure 2-8 BER Comparison between planar and NW channels with 20 and 30 nm gate lengths. BER calculated with the following two additional constraints are also shown for illustration: 1) all NCs within the gate region (FC) or 2) only NCs that are centered within the channel area (PC) have five electrons stored.

### 2.4.3. Templated Assembly of NC

NC placement can be regulated by polymer [25] or protein [26] lattice, and hence the NC size and position variation becomes negligible. However, the number density and vertical alignment with NW devices will still contribute to $\Delta V_{th}$ variations. Figure 2-9 shows the $V_{th}$ roll-off behavior and statistical error bars for an array of NCs orthogonally aligned with fixed inter-NC distance of 10 nm and NC diameter of 5 nm.

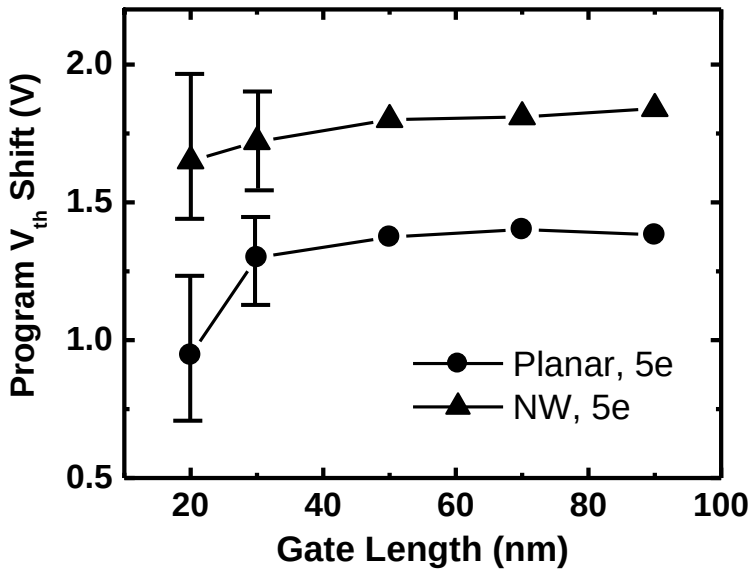



Figure 2-9 $V_{th}$ roll-off behavior with statistical error bars for the 3 nm diameter nanowire and planar devices. Each NC is charged with five electrons. NCs are orthogonally aligned with a fixed inter-NC distance of 10 nm and the NC diameter is 5 nm.

NW devices have superior control on the short-channel effect (SCE) even in sub-30 nm devices and larger $\Delta V_{th}$ for the same number of electrons stored in each NC, but we observe NW devices having similar $\Delta V_{th}$ fluctuation as the planar devices. Originally, the bottleneck effect [16] with decreasing channel width in the NW device is expected to eliminate the percolation leakage effect and increase mean memory

window as well as standard deviation. However, if we consider 3D fringing, $\Delta V_{th}$ fluctuation should be less severe in the NW device in comparison with previous semi-1D models [9, 16]. As illustrated in Figure 2-10, planar and 3 nm NW devices can have similar $\Delta V_{th}$ fluctuation. Although planar devices are less sensitive to NC number density variation, it lacks the channel-NC coupling enhancement effect in the NW devices.

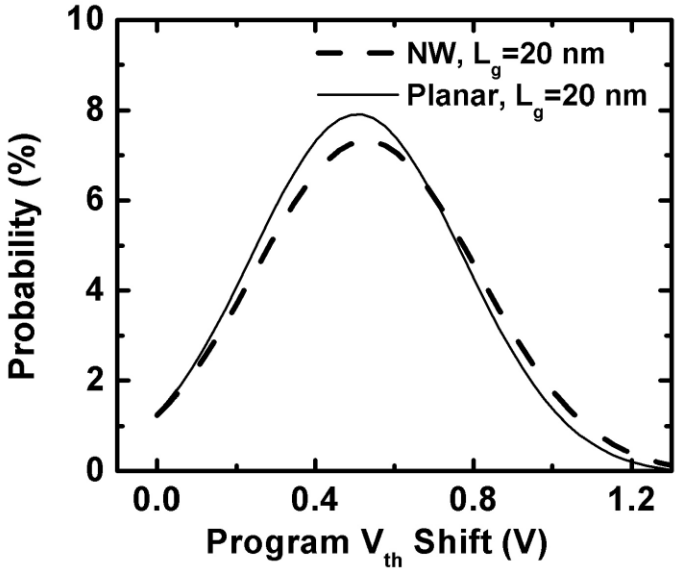



Figure 2-10 Gaussian-fitted curves to the $\Delta V_{th}$ distribution estimated by the Monte Carlo method for the planar (solid lines) and 3 nm nanowire devices (dash lines). Gate length is 20 nm and all NCs within the gate area have five electrons stored.

### 2.4.4. Self-Alignment of NC to Nanowire or Nanotube Channels

Previous work has demonstrated that carbon nanotube (CNT) devices can achieve self-aligned (SA) NC to the CNT [18] by surface energy preference. Figure 2-11 compares planar to SA NW devices with average number density of $10^{12}$ $cm^{-2}$ near the channel area. With NC diameter larger than that of the NW, NC to channel coupling is dominant due to the fringing field enhancement. Number density variation on $\Delta V_{th}$ becomes less severe with increased density near the channel surface area. Thus, we

observe a higher $\mu(\Delta V_{th})$ and smaller $\sigma(\Delta V_{th})$, which suggests SA NW devices can be the device candidate to achieve small BER.

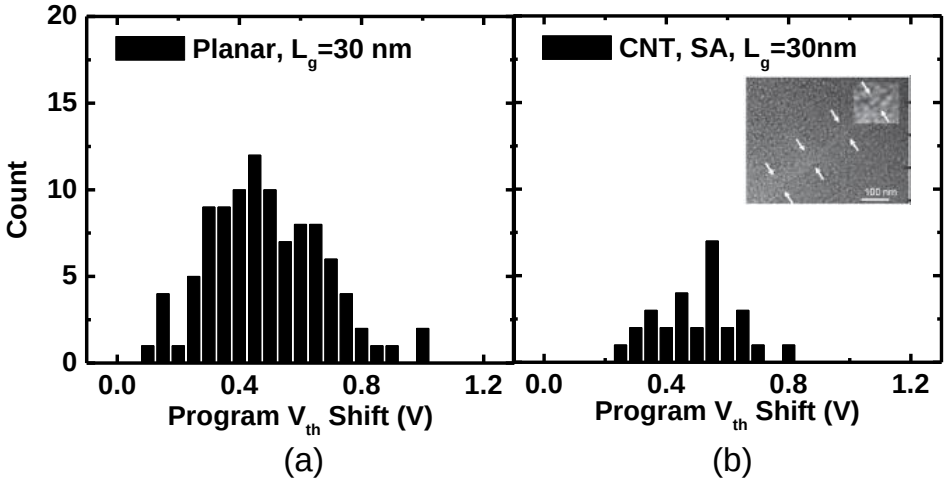



Figure 2-11 Monte Carlo simulation results of (a) planar (100 cases) and (b) 3 nm diameter self-aligned nanowire devices (25 cases). Gate length is set at 30 nm. Inset shows an SEM image of self-aligned NC to carbon nanotubes, where NCs are concentrated near the channel area.

## *2.5 Conclusion*

We have demonstrated the importance to include 3D electrostatics and channel percolation in metal NC memory statistical metrology and examined BER in various channel structures for scaling prediction. Contrary to previous semi-1D models, $\Delta V_{th}$ fluctuation is mainly due to number density variation and less sensitive to NC diameter variation within the range of 6.1 ± 1.2 nm. In addition, field-enhancement effect from NCs away from the channel has noticeable effect on devices with small width/length ratios. NW devices benefit from the field enhancement and the bottleneck effect to achieve higher threshold voltage shift, but with diminishing return as the gate area is scaled down even with templated NC placement. Self-alignment of

NC to NW shows strong promise in both increasing memory windows and controlling $\Delta V_{th}$ fluctuation.

### 2.5.1. Reflection

There is an inherent tradeoff between the simulation time and computation effort. Depending on the model complexity, often times certain assumptions must be made. In addition, having an intuition for the solution will help the user determine the minimum mesh density required and the most suitable solver to reach a convergent solution in a timely fashion.

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# CHAPTER 3

# INTEGRATION OF SELF-ASSEMBLED REDOX MOLECULES IN FLASH MEMORIES

## *3.1 Abstract*

Self-assembled monolayers (SAMs) of either Ferrocenecarboxylic acid (FcCOOH) or 5-(4-Carboxyphenyl)-10,15,20-triphenyl-porphyrin-Co(II) (CoP) with high-$\kappa$ dielectric were integrated into the Flash memory gate stack. The molecular redox states are used as charge storage nodes to reduce charging energy and memory window variations. Through the program/erase (P/E) operations over tunneling barriers, the device structure also provides a unique capability to measure the redox energy without the strong orbital hybridization of metal electrodes in direct contact. Asymmetric charge injection behavior was observed, which can be attributed to the Fermi-level pinning between the molecules and the high-$\kappa$ dielectric. With increasing redox molecule density in the SAM, the memory window exhibits a saturation trend. Three programmable molecular orbital states, $CoP^{0}$, $CoP^{1-}$, $CoP^{2-}$, can be experimentally observed through a charge based nonvolatile memory structure at room temperature. The electrostatics is determined by the alignment between the HOMO (highest occupied molecular orbital) or LUMO (lowest unoccupied molecular orbital) energy levels and the charge neutrality level (CNL) of the surrounding dielectric. Engineering the HOMO-LUMO gap with different redox molecules can potentially realize a multi-bit memory cell with less variation.

## *3.2 Introduction*

Flash memory device structures with discrete charge storage such as nanocrystals (NC) and dielectric traps are potential candidates for continuous memory scaling by maintaining coupling ratio and reducing cross-talk in conventional floating gate devices. Metal NC embedded in high-$\kappa$ dielectric [1] has been proposed to improve low-voltage program/erase (P/E) efficiency by the 3D field enhancement effect [2]. The metal work function also provides additional offset to the Si band edges to prolong retention. However, non-uniformity in NC size and density raises concerns of the parametric yield for aggressive scaling [3]-[4]. Charge storage in dielectric traps is also vulnerable to trap density and energy variations.

In comparison, a combination of the top-down lithography and the bottom-up molecule self-assembly processes can offer a uniform charge density and possible stable multi-level storage in a single memory cell [5]. The mono-disperse nature of the molecular orbitals (MOs) can potentially reduce cell variations, while the distinct energy levels may enable stepwise charging for precise control of each memory state. By attaching redox molecules as a floating gate in the CMOS structure, one also creates a high-impedance non-amperometric electrode for probing the molecular redox states, in contrast to the low-impedance connections used in cyclic voltammetry (CyV) [6-9]. Previous studies have shown capacitance and conductance peaks associated with the charging and discharging of the carriers stored at the molecular orbitals [7] and CyV hysteresis owing to the reduction/oxidation of molecules attached to the $SiO_2$ surface [6, 8-9].

Compared to the CyV measurements where the insulating barrier was only deposited on one side [6, 9], the new structure provides insulating barriers above and

below the molecules, which further lessen the possibility of orbital hybridization from the gate. A strong coupling between the electrode and the molecule may lead to molecule-independent switching behavior and modification of the intrinsic spacing of the energy levels [10], which makes it difficult to study the molecule-specific behaviors. Furthermore, the lack of insulating capping layer in CyV compromises carrier retention. An additional shortcoming with the CyV method is the slow time scale due its reliance on ionic movement. The operation speed can be enhanced significantly with an all-electron conduction mechanism in the proposed structure. Further, the specifically tailored redox molecules can be self assembled as a monolayer in current CMOS technology through the chosen functional end group, where the discrete levels of the molecular orbitals can be preserved as discrete memory states.

In this study, we have integrated various molecules with high-$\kappa$ dielectric in an otherwise standard Flash memory gate stack. We report the charge retention and P/E characteristics. We further confirm that porphyrin molecules have the thermal budget that can withstand post-metal gate annealing [11] – an important requirement for CMOS-compatibility. Compared with the previous studies [6-9], we were able to confirm interaction with multiple states of redox-active molecules, instead of interface traps.

## *3.3 Device Fabrication*

The metal-oxide-semiconductor (MOS) capacitor structure, similar to that used in Flash memory devices [12-13], with redox molecules embedded in the control dielectric, was fabricated. Two types of redox molecules were integrated: ferrocenecarboxylic acid (FcCOOH) and 5-(4-Carboxyphenyl)-10,15,20-triphenyl-

porphyrin-Co(II) (CoP). The schematics of the devices with FcCOOH (S1) and CoP (S2) molecules are illustrated in Figure 3-1. Both molecules are stable in air with FcCOOH and CoP exhibiting two and three stable redox states, respectively.

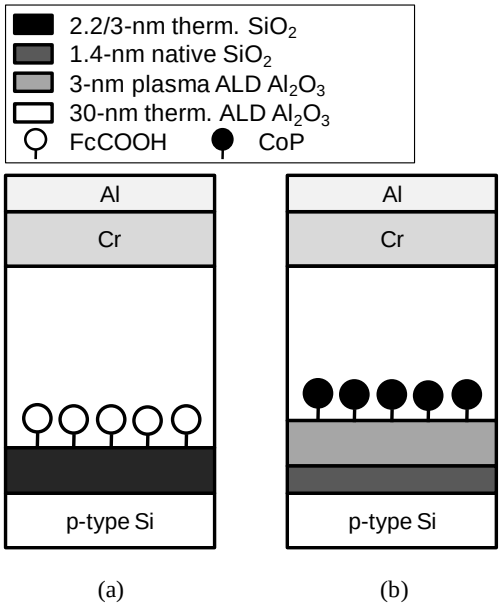



Figure 3-1 Schematics of the MOS capacitor structure with ferrocenecarboxylic acid (FcCOOH) (S1) and (b) CoP (S2) molecules integrated as storage nodes.

We followed a self-assembled monolayer (SAM) formation process similar to previous literature [9], utilizing the carboxyl functional group on the OH-terminated surface. For S1, after 2.2 nm or 3.0 nm dry thermal oxide growths on a p-Si(100) substrate, the wafer was immersed in a solution of dimethyl formamide (DMF) with 1 mM FcCOOH. The solution was kept at 80 $^{o}$C for 120 minutes under Argon environment during the self-assembly process. For S2, the wafer was first placed in a 1% HF solution to remove the native oxide followed with DI water rinse/$N_2$ blow dry and then immediately loaded into the atomic layer deposition (ALD) chamber. After 3 nm of $Al_2O_3$, the wafer was immersed in a 1 mM CoP solution of DMF at room temperature for 24 hours under Argon environment. It is worthwhile to note that

native $SiO_2$ forms readily in air. A native oxide of ~ 1 nm was present before $Al_2O_3$ growth on a separate test sample, which went through identical HF etch process, measured by ellipsometry. Prior to the growth of the control dielectric, the native $SiO_2$ was measured to be ~ 1.4 nm on our test sample with no molecules present. The native $SiO_2$ possibly formed during DI water rinse/$N_2$ dry after etching by HF and the initial cycles of thermal $Al_2O_3$ deposition. The surface density has been estimated to be around $1.0 \times 10^{14}$ $cm^{-2}$ and $0.45 \times 10^{14}$ $cm^{-2}$ for FcCOOH and CoP SAMs, respectively [6], assuming a full surface coverage. Furthermore, the thickness of FcCOOH and CoP SAM measured by ellipsometry were in the range of 0.9-1.2 nm and 1.5-1.6 nm, respectively, which is in good agreement with previous estimate where the thickness is estimated to be 0.8 nm and 1.5 nm by impedance spectroscopy [8]. After the self-assembly process, DMF was used to rinse the wafer to remove any residual molecule that is not covalently bonded to the surface. The SAM was covered by 30 nm of ALD $Al_2O_3$ grown by the reaction of trimethylaluminum and $H_2O$ at 110 $^oC$. The Cr/Al control gate was then deposited and patterned, followed by $H_2/N_2$ forming gas anneal at various conditions.

We report the molecule structure of the FcCOOH molecule and the CoP molecule in Figure 3-2. $t_m$ is the approximate distance from the attachment site to the redox-active transition metal, where $t_M$ is the thickness of the molecule. The dummy molecules, exhibiting no redox states, were added in the control splits for various surface density coverage of the redox-active molecules. Dummy molecules were selected based on structural similarity to the *active* molecules to ensure solubility of the dummy molecule in the deposition solution, and to promote effective mixing of the dummy and active molecules on the surface.

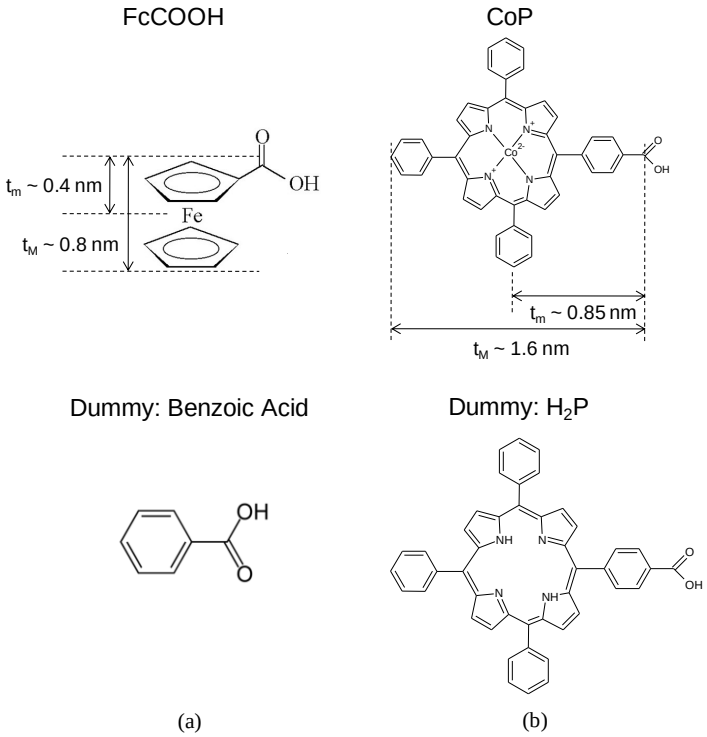



Figure 3-2 Molecular structure of FcCOOH, CoP and the respective dummy molecules used to control surface coverage density of the redox-active molecules. The approximate distance from the attachment site to the central transition-metal, $t_m$, and thickness as-deposited on the surface, $t_M$, are illustrated for each redox-active molecule.

The dummy molecule for FcCOOH is the benzoic acid (Bz), where 1:100 mixing is derived from 0.01 mM of FcCOOH and 1 mM of Bz. Assuming the 1:100 mixing ratio in the bulk solution leads to a 1:100 mixing of FcCOOH:Bz on the attachment surface, the density corresponds to an inter-molecule spacing of ~ 5.8 nm for FcCOOH. We estimate the minimum inter-molecule distance of 0.1 eV Coulomb blockade as:

$$\Delta E = \frac{1}{4\pi\varepsilon_r\varepsilon_0}\frac{q_1 q_2}{r} \le 0.1eV \qquad (1)$$

$$r \ge 5.75nm$$

where $\Delta E$ is the energy shift due to repulsion force from the neighbor molecules, $q_1$ and $q_2$ are the charge stored in the redox-active molecules, $r$ is the inter-molecule distance, and $\varepsilon_r$ and $\varepsilon_0$ are the relative and vacuum permittivity. Here, we assume $\varepsilon_r$ of Bz to be 2.5. CoP was mixed with 5-(4-Carboxyphenyl)-10,15,20-triphenyl-21,23H-porphyrin ($H_2P$), which acts as the dummy molecule, at a 1:20 ratio.

## *3.4 Results and Discussion*

Figure 3-3 shows the X-ray photoelectron spectroscopy (XPS) measurement on the samples of as-deposited FcCOOH and CoP SAMs. The $2p_{1/2}$ and $2p_{3/2}$ electron configuration corresponding to the orbital binding energy peaks of iron and cobalt can be clearly observed for the FcCOOH and the CoP SAMs, respectively. Since ferrocene is an organometallic compound that contains two cyclopentadienyl rings bound to a central iron, the observation of peaks at binding energies characteristic of the Fe $2p_{1/2}$ and $2p_{3/2}$ levels is evidence of ferrocene on the tunneling oxide. Similarly, in the case of the CoP SAM, the characteristic cobalt binding energy peaks indicate the existence of CoP deposited on the $Al_2O_3$ surface.

The XPS features may also be used to estimate the absolute densities of the redox-active molecules [14]. To quantify the coverage density of the redox molecules chemisorbed to the oxide surfaces, we use XP spectra from the evaporated Au (not shown) on silicon substrate as a reference standard. The integrated intensity under the [Au(4f)] feature from the standard is proportional to $\sigma_{Au} N_{Au} \lambda_{Au} T(E_{Au})$, where $\sigma_{Au}$, $N_{Au}$ = 5.88 × $10^{22}$ atoms/$cm^3$ [15], $\lambda_{Au}$=1.78 nm [16], and $T(E_{Au})$ are the photoelectron cross section, atomic density, inelastic mean free path, and analyzer transmission, which is inversely proportional to the photoelectron kinetic energy. If we assume the redox molecules form a finite thickness monolayer on the surface, $d_{SAM}$, with atomic

density $N_{SAM}$, and $d_{SAM}$ << inelastic mean free path of SAM $\lambda_{SAM}$, the area under the Fe(2p) and Co(2p) features will then be proportional to $\sigma_{Fe}\, N_{SAM}\, d_{SAM}\, T(E_{Fe}) / \cos\theta$ and $\sigma_{Co}\, N_{SAM}\, d_{SAM}\, T(E_{Co}) / \cos\theta$, where $\sigma_{Au} / \sigma_{Fe} \sim 1.04$ and $\sigma_{Au} / \sigma_{Co} \sim 0.89$ [17] for Fe(2p) and Co(2p), respectively, and $\theta = 55°$ is the photoelectron takeoff angle from surface normal. With these assumptions, the surface density, $N_{SAM}\ d_{SAM}$ (molecules/cm$^2$), of FcCOOH and CoP can then be calculated to be $1.58 \times 10^{14}$ and $3.6 \times 10^{13}$ molecules/cm$^2$, respectively, for SAM layers undiluted with dummy molecules, which agree well with previous estimation by cyclic voltammetry (CyV) [6]. Considering the assumptions that were made with the estimation method and the background noise, the absolute accuracy is approximately ±35%.

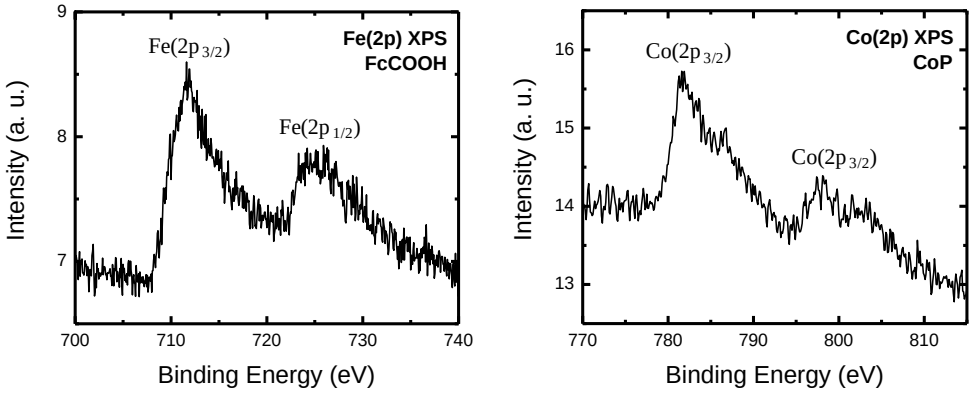



Figure 3-3 X-ray photoelectron spectroscopy (XPS) data of (a) FcCOOH SAM deposited on thermally grown $SiO_2$ and (b) Cobalt-Porphyrin (CoP) SAM deposited on ALD $Al_2O_3$. For XPS studies, no dummy molecules were used for preparing the SAM solution. The SAM solution concentration of FcCOOH and CoP is 1mM.

Furthermore, the contact angles measured before and after FcCOOH attachment were $10^o$ and $80^o$, respectively, which indicates that the film went from a

hydrophilic oxide to more hydrophobic organic surface. For CoP, the contact angles were 31 $^{o}$ and 55 $^{o}$ before and after the self-assembly process, respectively. Our results from XPS, ellipsometry and contact angle measurements suggest that a monolayer of FcCOOH and CoP molecules were formed on the $SiO_2$ and $Al_2O_3$ surfaces, respectively. Furthermore, CyV was performed with 2mM of FcCOOH in acetonitrile containing 0.1 M of tetrabutylammoniun hexafluophosphate ($TBAPF_6$) as supporting electrolyte as illustrated in Figure 3-4. The current peaks are associated with the oxidation (negative current) and reduction (positive current) of the molecules. One reversible redox state was observed at +0.71 V vs. the Ag/AgCl reference electrode.

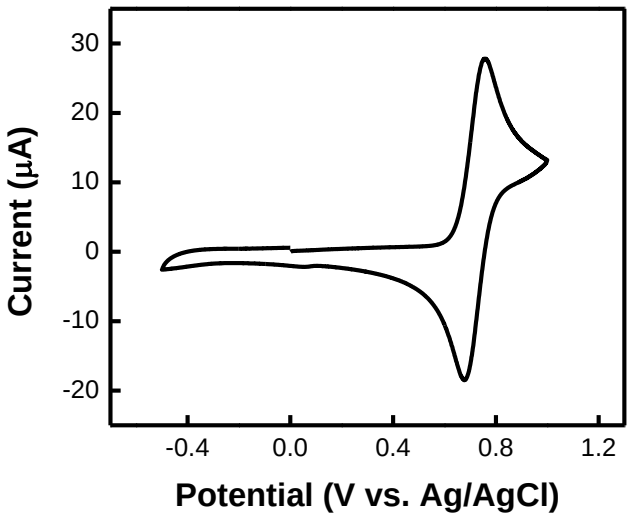
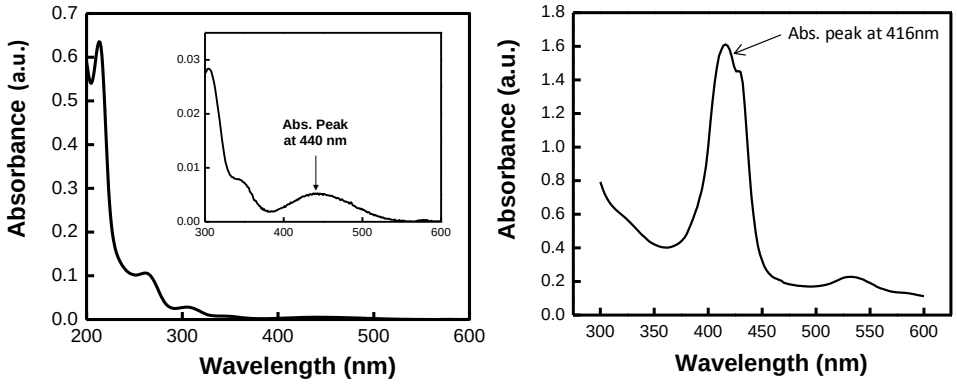



Figure 3-4 Cyclic voltammetry of 2 mM FcCOOH in acetonitrile containing 0.1 M tetrabutylammoniun hexafluophosphate (TMBAPF6) as supporting electrolyte. Ag/AgCl was used as the reference electrode.

Apart from this, from the resonant peak in the UV/Vis absorption spectrum shown in Figure 3-5, the HOMO-LUMO energy gap can be estimated by the de Broglie equation, $E=hc/\lambda$, where $c$ is the speed of light in a vacuum and $E$ is the energy gap



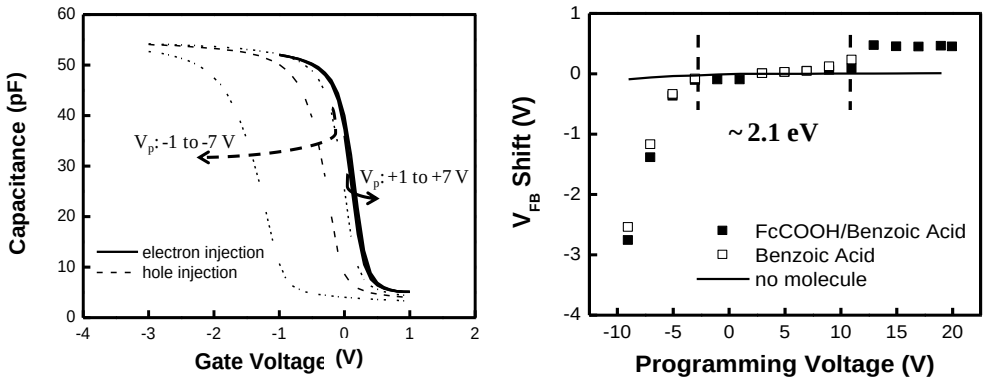

(a) (b)

Figure 3-5 UV/Vis absorption spectrum of (a) FcCOOH in acetonitrile and (b) CoP in dimethyl formamide (DMF). Deduced from the maximum absorption peak of the lowest energy band at 440 nm, the spectroscopic HOMO-LUMO energy gap is estimated to be ~2.8 eV and ~2.65 eV for FcCOOH and CoP molecules, respectively.

that corresponds to the resonant wavelength, $\lambda$. The spectroscopic HOMO-LUMO energy gap was estimated to be ~2.8 eV and ~2.65 eV for FcCOOH and CoP molecules, respectively, which matches well with the *ab initio* calculations by density functional theory (DFT) [18-19]. The HOMO/LUMO energy levels are estimated by DFT to be about -4.51/-1.72 eV for the FcCOOH molecule, and –4.8/–2.2 eV for the CoP molecule [18-19].

Consider the electrical characterization of CoFeOH sample, for which, the high frequency capacitance-voltage (HFCV) measurements in Figure 3-6(a) were taken by applying stress voltages on the control gate for 5 seconds to ensure that the program operation reaches the steady state, followed by sweeping the voltage from the positive to negative direction for studying electron injection and negative to positive for hole injection from the silicon substrate. All subsequent HFCV measurements performed at 10 K were under a light source to promote minority carrier generation. For this sample, 2.2 nm of thermal oxide was grown as the tunneling oxide with a forming gas

anneal performed at 400 $^{o}$C for 30 minutes. The surface coverage ratio is assumed to be identical to the bulk solution ratio of 1:100 between FcCOOH and Bz (as a dummy molecule). First, we notice that at small programming voltages, hole injection showed a large memory window while electron injection is negligible, which indicates that hole injection is preferred when FcCOOH SAM is embedded in $Al_2O_3$. Also worth noticing is the CV stretch-out at higher programming voltages, which can be attributed to charge leakage back to the silicon substrate. Figure 3-6(b) shows the amount of flatband shift ($\Delta V_{FB}$) as a function of programming voltage extracted from the HFCV measurements. The participation of both electron and holes is evident from the linear increase in $\Delta V_{FB}$ by positive and negative writing, respectively.




(a) (b)

Figure 3-6 (a) High frequency *CV* (HFCV) measurements and (b) $\Delta V_{FB}$ as a function of the programming voltage at 10 K and room temperature for capacitors with FcCOOH molecules. The mixture between FcCOOH and Bz has a 1:100 ratio. Device was annealed at 400 $^{o}$C for 30 min. Carrier injection tests were carried out by applying stress voltages for 5 s before each *CV* sweep. The programming voltage ($V_p$) for electron and hole charging is applied from ±1 V to ±7 V in 2 V increment. Subsequently, the gate voltage is swept from accumulation to inversion for electron charging and inversion to accumulation for hole charging. The size of the MOS capacitor is 150 ×150 $\mu$m$^2$.

The injected charges have three possible storage sites: dielectric traps of $Al_2O_3$, traps nearby the $Al_2O_3$/FcCOOH interface, and FcCOOH itself to reduce/oxidize the molecule. Since the sample without any molecules embedded in the gate stack has shown negligible $\Delta V_{FB}$ for programming voltage of -10V to +20V, charges are not likely to be stored in dielectric traps of $Al_2O_3$. A linear increase in $\Delta V_{FB}$ with respect to the programming voltage is an indication of charges being stored at the interface states whereas a staircase behavior has been regarded as a signature of charge storage in the redox molecules, which has discrete energy levels corresponding to the various molecular the orbital [5]. Saturation at high positive biases can be a result of Frenkel-Poole (F-P) leakage through the control dielectric or the Coulomb blockade effect [5]. The charge neutrality level (CNL) of $Al_2O_3$ deposited by ALD is around –5.2 eV [20]. The CNL can be regarded as a local Fermi level of the interface states or metal-induced gap states (MIGS) [21], which are dangling bonds that disperse across the band gap of the dielectric. It is evident that the energy level alignment between the molecular orbitals and the surrounding dielectric's CNL is crucial for determining the memory properties [5, 20-21]. Coulomb staircase behavior at negative gate biases was not observed for several possible reasons. First, holes have a preference to relax to the CNL, which is slightly above the HOMO energy level. Second, upon interface formation, the energy level may have been shifted due to fractional charge transfer at the interface. A further evidence comes from the fact that the control sample with only Bz molecules also results in hole storage with slightly smaller memory window than samples with FcCOOH molecules. Knowing that Bz molecules do not exhibit any redox states, injected holes are most likely stored in the interfacial traps created by the dangling bonds. This indicates that both FcCOOH and Bz molecules generate traps at the dielectric interface as one would expect, which are the preferential sites for hole storage.

Moreover, the preference for the hole storage can be further explained by the Fermi-level pinning theory [5, 13, 22]. Figure 3-7 illustrates the band diagram with FcCOOH molecule as the storage node. Electron injection is forbidden at low programming voltages because electrons must have an energy greater or equal to $E_{LUMO} - E_c + \Delta E_{ch,e} = 2.35\ eV + \Delta E_{ch,e}$, where $E_c$ is the silicon conduction band and $\Delta E_{ch,e}$ is the single electron charging energy. Upon injection, electrons would preferentially relax to the interface traps near the CNL with lower energy. From the energy alignment, the energy required for the hole injection is $E_v - E_{HOMO} + \Delta E_{ch,h} = -0.66\ eV + \Delta E_{ch,h}$, where $E_v$ is the silicon valence band and $\Delta E_{ch,h}$ is the single hole charging energy. Thus the hole storage is energetically favorable than the electron storage.

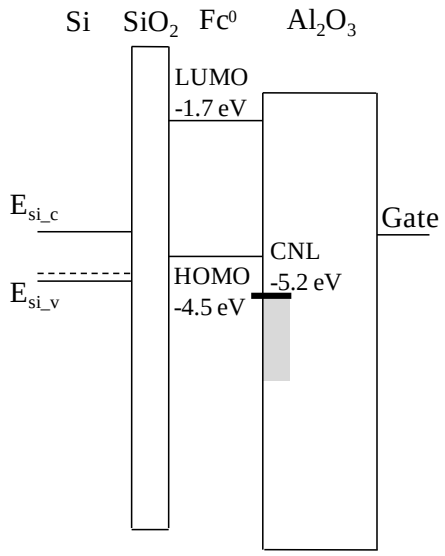



Figure 3-7 Energy band diagram representation of the capacitor structure with FcCOOH molecules. The charge neutrality level (CNL) of $Al_2O_3$ is shown and FcCOOH molecule is assumed to be in its neutral state.

Apart from this, Figure 3-8 illustrates the change in memory window for different mixture ratio between FcCOOH and Bz at negative gate biases. For this sample, the forming gas anneal was performed at 300 $^oC$ for 90 minutes with 3 nm of thermal $SiO_2$

as the tunneling oxide. The amount of $\Delta V_{FB}$ increases proportionally with increase in the density of FcCOOH molecules in the SAM, which suggests that increasing the number of FcCOOH molecules increases the number of sites for hole storage. This also confirms our previous argument, derived from the energy band diagram, that holes have preference to be stored at interfacial trap sites created by FcCOOH molecules.

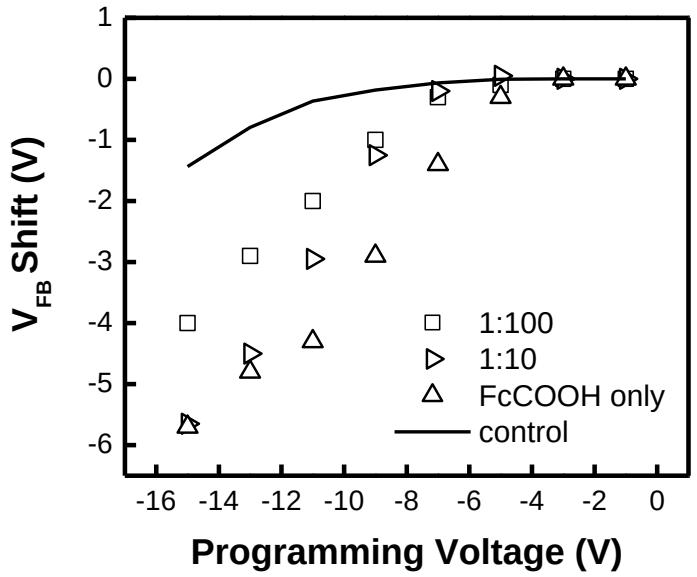
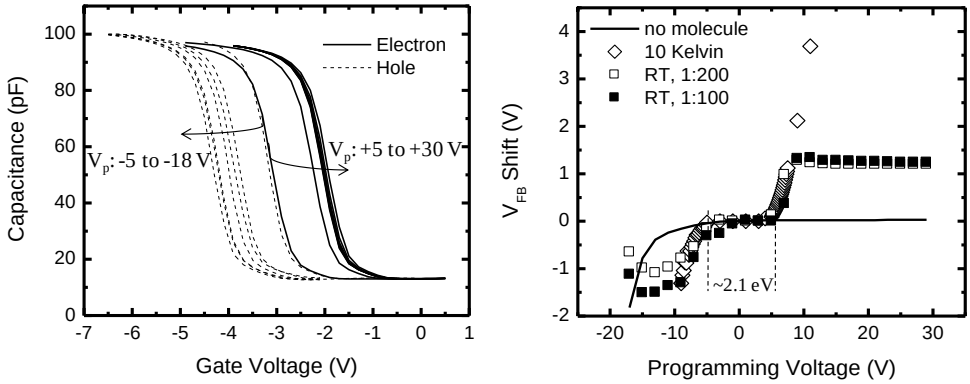



Figure 3-8 $\Delta V_{FB}$ as a function of programming voltage for devices with FcCOOH molecules mixed with Bz molecules at mixture ratios of 1:100, 1:10, and FcCOOH molecules only in the deposition solution. A 90 min forming gas anneal was performed at 300 $^{o}$C. Measurements taken on the sample with no molecules are also shown for comparison.

To pinpoint the cause of $\Delta V_{FB}$ saturation at positive gate biases and the charge storage mechanism, we decreased the density of FcCOOH molecules and performed HFCV measurements at cryogenic temperatures. A new batch of samples (with 3 nm of $SiO_2$ as the tunneling oxide) were annealed at 200 $^{o}$C for 60 minutes and the

mixture ratios between FcCOOH and Bz molecules were 1:100 and 1:200 (*e.g.*, 0.005 mM of FcCOOH to 1 mM of Bz), which translates to the inter-molecular distance for FcCOOH of 5.8 nm and 8.2 nm, respectively, assuming the surface coverage ratio is the same as the bulk solution for preparing the SAM. Concentration of FcCOOH molecules is reduced to moderate the coulomb repulsion force, which could affect the charging potential of neighboring molecules. A lower annealing temperature was chosen to avoid molecule degradation.

In Figure 3-9, HFCV and $\Delta V_{FB}$ as a function of the programming voltage are shown.




(a) (b)

Figure 3-9 (a) HFCV and (b) $\Delta V_{FB}$ as a function of the programming voltage at 10 K and room temperature for FcCOOH molecules. The two mixture ratios between FcCOOH and Bz molecules are 1:200 and 1:100 with a tunneling oxide of 3 nm thermal $SiO_2$. A 60 min forming gas anneal was performed at 200 $^{o}$C. Measurements taken on the sample with no molecules are also shown for comparison. HFCV measurements were taken at 100 KHz. The programming voltage ($V_p$) for electron and hole charging is applied from +5 V to +30 V and -5 V to -18 V, respectively. Subsequently, the gate voltage is swept from accumulation to inversion for electron charging and inversion to accumulation for hole charging. The size of the MOS capacitor is 200 × 200 $\mu$m$^2$.

From Figure 3-9(a), we notice that the asymmetric injection and CV stretch-out is no longer present, possibly due to interface dipole formation, which shifted the band alignment. At 10 K, the amount of $\Delta V_{FB}$ increases linearly in proportion to the positive gate biases while a saturation behavior was observed at room temperature. In addition, the saturation voltage is approximately the same for the two different mixture ratios. Both the temperature and concentration dependences suggest that the saturation behavior originate from F-P conduction through the control dielectric at room temperature [5], which is a non-ideal situation in our present process integration.

$\Delta V_{FB}$ can be described by the relation:

$$\Delta V_{FB} \approx \frac{Q}{C_{cont}} \approx \frac{q \times n \times N}{C_{cont}} \qquad (2)$$

where $Q$, $q$, $n$, $N$ and $C_{cont}$ are the total stored charge density in the molecules, the elemental charge, the number of charges per molecule, the number density of the molecule, and the capacitance of control oxide, respectively. $\Delta V_{FB}$ shift is approximately 1.3 V in Figure 9, and from Eq. (2) we obtain a trap density of $2.0 \times 10^{12}$ $cm^{-2}$. Once all the traps are occupied, any additional electron would need to overcome the repulsion force from the electrons stored in the lowest energy state of interface traps to enter the molecular orbital. As we increase the gate bias further, the electrons would gain enough energy against the repulsion force, but tends to leak out of the control dielectric by F-P conduction.

There is one more interesting observation. Modeling the molecule as a thin dielectric layer, we can obtain the total voltage drop from the $SiO_2$/Si interface to the central redox-active atom, $V_{ch}$, as:

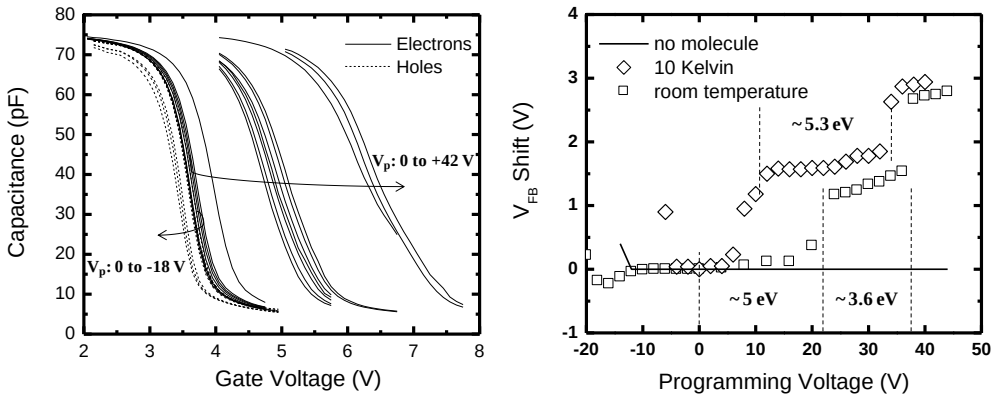
$$V_{ch} = \frac{t_{tunn} + \frac{\varepsilon_{ox}}{\varepsilon_M} t_m}{t_{tunn} + \frac{\varepsilon_{ox}}{\varepsilon_M} t_M + \frac{\varepsilon_{ox}}{\varepsilon_{cont}} t_{cont}} V_G \qquad (3)$$

$t_{tunn}$, $t_{cont}$, and $t_m$ are the tunnel oxide thickness ($SiO_2$), physical thickness of the $Al_2O_3$ control dielectric, and the approximate distance from the attachment site to the redox-active transition metal, as illustrated in Figure 3-2. $t_m$ is estimated to be 0.5 $t_M$. $\varepsilon_M$ and $t_M$ are the dielectric constant and thickness of the molecule, respectively, assuming that the silicon channel is under inversion or accumulation. $\varepsilon_M$ and $t_M$ were determined in previous reports through impedance characterization to be 2.4 and 0.8 nm, respectively [8]. $\varepsilon_{cont}$ = 9 and $\varepsilon_{ox}$ = 3.9 are the dielectric constants of the control and tunneling oxide, respectively. In Figure 3-6(b) and Figure 3-9(b), the total blockade voltage can be calculated using Eq. (3) to be 2.1 eV in both cases, assuming the energy required to initiate charge injection is approximately the same as $eV_{ch}$, with a shift in the absolute value for different annealing conditions. The shift indicates the slightly different band alignment is due to the interfacial dipoles and fixed charge at the molecule/$Al_2O_3$ interface, but the HOMO-LUMO energy gap is identical in both cases. Depending on the annealing condition, the density of interface traps will vary as a function of energy, which leads to the difference in flatband voltage. However, the consistency in the blockade voltage suggests that the molecular orbital energy spacing is preserved within the dielectric environment.

If the molecule density is high enough to enable free lateral transport (continuous floating gate), $\Delta E_{ch}$ will not be significant and the discrete energy levels of the molecule would not be observable. The dilute FcCOOH/Bz samples have total blockade energy of 2.1 eV, which indicates that the charging energy remains

negligible after diluting the concentration of FcCOOH molecules. Therefore, it is likely that the carriers were injected into the interfacial traps since significant trap states are involved at the FcCOOH/$Al_2O_3$ or Bz/$Al_2O_3$ interface. The constant plateau regions suggest that the HOMO-LUMO energy gap acts as the energy barrier that carriers must overcome to initiate electron/hole injection. However, carriers quickly relax to surrounding interface states to favor the lower CNL energy.

Next, we consider the electrical characterization for the CoP redox-active molecules. Figure 3-10 shows the (a) HFCV and (b) memory window as a function of programming voltage.




(a) (b)

Figure 3-10 (a) HFCV and (b) $\Delta V_{FB}$ as a function of the programming voltage at 10 K and room temperature for the device with CoP molecules. The mixture ratio between CoP and $H_2P$ is 1:20. A 30 min forming gas anneal was performed at 400 $^oC$. Measurements taken on the sample with no molecules are also shown for comparison. HFCV measurements were taken at 100 KHz. The programming voltage ($V_p$) for electron and hole charging is applied from 0 V to +42 V and 0 V to -18 V, respectively. Subsequently, the gate voltage is swept from accumulation to inversion for electron charging and inversion to accumulation for hole charging. The size of the MOS capacitor is 200 × 200 $\mu m^2$.

Gate injection prohibits hole injection beyond programming voltages below -18 V. On the contrary, electron injection shows two distinct levels of Coulomb staircase, which is in good agreement with the previous measurements using CyV [6-9]. Assuming full coverage density of $4.5 \times 10^{13}$ $cm^{-2}$ and 1:20 dilution of deposition solution leads to equal dilution of SAM, the 1:20 mixture ratio with $H_2P$ translates to a CoP number density of about $2.2 \times 10^{12}$ $cm^{-2}$ and a flatband voltage shift of about 1.32 V for the single electron injection. This value matches well with the amount of flatband voltage shift observed in Figure 3-10, which is approximately 1.4 V at room temperature and 1.6 V at 10 K. At room temperature, the large leakage between the carrier storage sites and the gate, possibly through hopping, prevents an efficient charging of the CoP molecules. Contrarily, measurements that were taken at 10 K also show Coulomb staircase behavior, but carrier storage begins at lower programming voltages due to the elimination of F-P leakage. It is worthwhile to note that the initial flatband voltage is ~ +3.5V, which differs from an ideal p-type MOS stack, which exhibits a flatband voltage of ~ -0.9V. The difference in flatband voltage is from the large amount of fixed charge created at the molecule-$Al_2O_3$ interface due to the non-ideal growth surface.

Figure 3-11 illustrates the energy band diagrams (a) before and (b) after depositing $Al_2O_3$ as the control dielectric on top of the molecules. The HOMO and LUMO energy levels for neutral $CoP^0$ were estimated by DFT calculation [19], whereas the CNL of ALD $Al_2O_3$ is -5.2 eV. According to the HOMO-LUMO energies of $CoP^0$ and CNL, electrons have the energy preference to relax to the CNL and Coulomb staircase would not be observed before the control dielectric is deposited. On the other hand, the interface dipole formation at the CoP and $Al_2O_3$ interface can lead to a different thermal equilibrium state, likely the mono-cation ($CoP^{1+}$), established by hole transferring from the interface states into $CoP^0$.

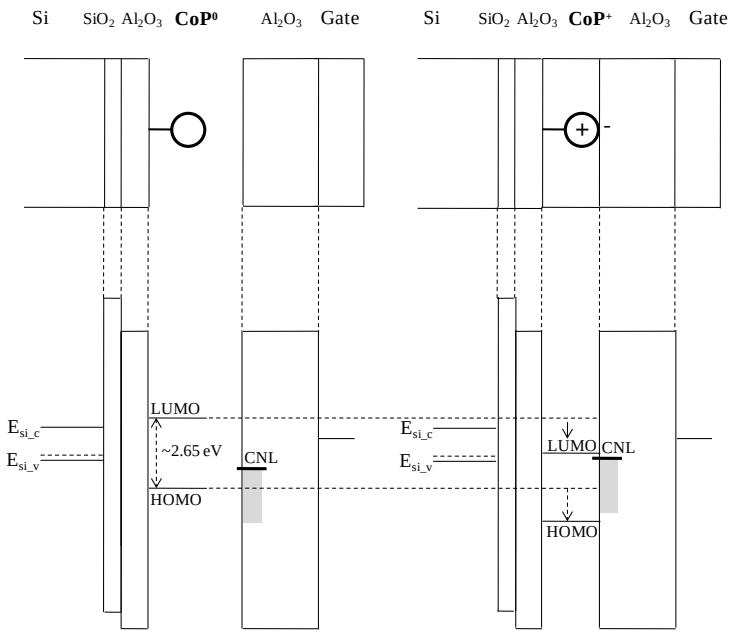



Figure 3-11 Energy band diagram at thermal equilibrium states (a) before and (b) after CoP molecule is in contact with the surrounding dielectric. The CNL and density of states are determined by the oxide's atomic configuration, which are sensitive to composition stoichiometries and deposition surface. The figure is not drawn to scale. The electron-filled interface states are indicated as the shaded regions. The HOMO-LUMO energy gap is estimated from the UV/Vis absorption spectra to be ~2.65 eV.

In addition, electron injection to the LUMO energy level is evident from the Coulomb staircase. Therefore, we expect the CNL to be in close proximity with LUMO so that injected carriers will not have the tendency to relax to the interfacial trap states. Electron injection into the $CoP^{1-}$ states to become dianion ($CoP^{2-}$) is not favorable until the LUMO energy is one $\Delta E_{ch,e}$ below the silicon conduction band edge, which corresponds to the 5 eV blockade voltage at room temperature. Sequential electron injection can be stable in the orbital states, as long as the leakage back to the substrate is not severe. The single-electron charging energy can be calculated by:

$$\Delta E_{ch,e} = \frac{q^2}{C} \qquad (4)$$

where $C$ is the self-capacitance of the storage node. However, the charging energy can only be estimated using a detailed calculation considering the complex geometry of the redox molecule embedded in the dielectric, which is not performed here. Instead, we will calculate the charging energy by first determining the self-capacitance by the following relation:

$$C_{self} = C_{CoP} \times A_{CoP} \qquad (5)$$

where $C_{self}$, $C_{CoP}$, and $A_{CoP}$ are the self-capacitance, capacitance per unit area and areal coverage of each CoP molecule. The capacitance per unit area can be extracted from impedance spectroscopy, which is 1.5 $\mu$F/cm$^2$ for the device with CoP molecules, estimated from previous literature [8]. $A_{CoP}$ is estimated from the amount of $\Delta V_{FB}$, which separates each reduced states.

In Fig. 10, the amount of $\Delta V_{FB}$ between the plateau regions is ~ 1.5 V at 10 K. From Eq. (2), we calculate the number density, $N$, to be 2.5 × 10$^{12}$ cm$^{-2}$, which translates to unit cell area, $A_{cell}$, of 4 × 10$^{-13}$ cm$^2$. Assuming a close pack self-assembled monolayer and the mixture ratio in liquid solution to be the same as the as-deposited molecules, the areal coverage of each CoP molecule, $A_{CoP}$ is 2 × 10$^{-14}$ cm$^2$, which can be calculated by the relation $A_{cell}/A_{CoP}$ ~ 20, considering the mixture ratio of 1:20 with $H_2P$. From Eq. (5), the self-capacitance of the CoP molecule can be readily calculated to be 3 × 10$^{-20}$ F.

From equation (4), the single-electron charging energy, $\Delta E_{ch,e}$, can be calculated to be ~ 5.6 eV. $\varepsilon_M$, $t_m$, and $t_M$, for CoP SAM are 2.5, 0.8 nm, and 1.6 nm, respectively. $t_{tunn}$ of the heterogeneous tunneling oxide is 2.7 nm. With these molecular parameters, the first plateau region in Fig. 10 has a blockade voltage of ~

5.3 eV at 10 K by Eq. (3), which is in good agreement with the single-electron charging energy of CoP molecule (5.6 eV).

Finally, Figure 3-12 shows the programming and retention characteristics for the FcCOOH and the CoP molecules. The retention time ($t_R$)/programming time ($t_P$) ratio of the device with CoP molecules is clearly improved as compared to the device with FcCOOH molecule as the storage node, possibly due to the large capture cross section of the redox molecules in comparison to the interfacial trap states in the device with FcCOOH molecules. Further improvement on program efficiency, voltage operation and retention is possible by adjusting the oxide thickness ratio, tunnel oxide thickness, surface coverage density of the molecules, integrating different redox molecules with various orbital energy levels, and improving the dielectric quality.

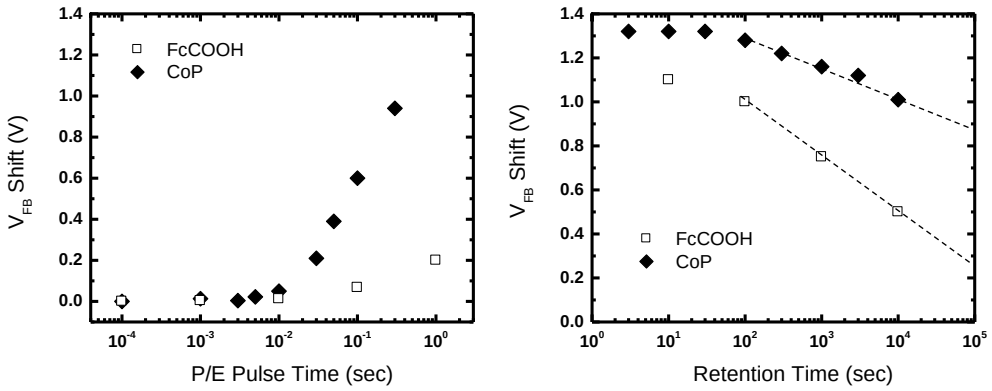



Figure 3-12 (a) Programming and (b) retention measurements of MOS capacitors with FcCOOH and CoP molecules. $\Delta V_{FB}$ was extracted from HFCV measurements. Devices were stressed for five seconds at +10 V before each retention measurement and programming tests were applied at +10 V. The sample with FcCOOH molecules has a tunneling oxide of 3 nm thermally grown $SiO_2$ and a 60 minute forming gas annealed was performed at 200 $^oC$. The mixture ratio between FcCOOH and Bz is 1:200. The sample with CoP molecules has a heterogeneous tunnel oxide composed of 1.4 nm native $SiO_2$ and 3 nm plasma ALD $Al_2O_3$.

## *3.5 Conclusion*

We have successfully integrated a monolayer of redox molecules in a Flash memory device structure using solution based self-assembly technique and demonstrated three programmable molecular orbital states of CoP molecule, including $CoP^{0}$, $CoP^{1-}$, and $CoP^{2-}$ at room temperature, which may help realize step charging into a multi-bit memory cell. For the device with FcCOOH molecules, the memory window increases proportionally with the density of the redox molecules, and the band offset of the HOMO-LUMO energy levels of FcCOOH molecule and the CNL of $Al_2O_3$ determines the preferred carrier storage sites. With the abundant choices of redox molecules and their inherent mono-dispersion in size and energy levels, our proposed approach can be readily integrated into a MOS-based nonvolatile memory cell and pave the wave for realizing multilevel molecular memories. Further, mixture of porphyrins with different transitional metal or integration of multi-state molecules [23] may offer additional molecular orbital states while maintaining small bit error rate.

### 3.5.1. Reflection

The molecules must be carefully characterized to obtain consistent surface coverage density and electrical properties. The molecular properties of an isolated molecule may be different after deposition and are highly dependent on the surrounding material. In addition to the non-ideal molecular/dielectric interface, the residual stress from $Al_2O_3$ deposition, chemical reaction with the oxide, degradation due to annealing and electrical stress, make it difficult to predict the energy alignment or charge storage properties of the redox molecules. Therefore, a thorough physical/electrical characterization with XPS, contact angle, ellipsometry, is absolutely necessary to verify the integrity of the molecules. FTIR could also provide

good insight for the bonding information, but the signal is too weak for a monolayer coverage even at low temperature conditions.

In terms of device fabrication, full MOSFET fabrication may be preferable over the MOS structure to ensure the programming speed is not limited by the minority carrier generation rate. To observe the step-charging effect, the programming pulse time needs to be long enough to ensure it reaches saturation, especially for thicker tunnel oxides. ALD $HfO_2$ was not a suitable control oxide due to the large number of interfacial states, which could not be passivated completely after forming gas annealing. For molecule-embedded MOS structures, metal deposition through shadow mask is recommended to avoid possible chemical contamination from photolithography and wet-etching.

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# CHAPTER 4
# REDOX MOLECULES FOR RESONANT TUNNELING BARRIER IN NONVOLATILE MEMORY

## *4.1 Abstract*

For better program/erase efficiency while maintaining retention, durable redox molecules were integrated into the flash memory gate stack to form resonant tunneling barrier (RTB) by either a hybrid organic/inorganic deposition or a simple solution-based layer-by-layer (LBL) method. In comparison with fullerene molecules [1], the proposed porphyrin has high number density and wafer-ready LBL process. Approximately six orders of magnitude improvement in electron retention to programming time ($t_R$ / $t_{PE}$) was observed for Au nanocrystal (NC) memory with a hybrid organic-inorganic tunnel barrier (HTB). With the LBL method, the $t_R$ / $t_{PE}$ improved by at least two orders of magnitude for both electron and hole carriers with P/E cycling endurance larger than $10^4$ cycles. Furthermore, the gate current is used to characterize the transport mechanism and study the electrical reliability of the organic layers. A better understanding of the charge storage and insulation properties of these organic barriers can improve future design integration on all-organic or hybrid molecular electronics.

## *4.2 Introduction*

Scaling conventional nonvolatile memory (NVM) is limited by the thickness of the tunnel oxide, which cannot scale below 7-8 nm due to gate leakage after stress [2]. In present nonvolatile memory technology, the retention to program/erase time ratio ($t_R$ / $t_{PE}$) is about $10^{12}$ – $10^{14}$. To achieve this enormous ratio, large Fowler-Nordheim

(F-N) tunneling current during program/erase operations and small direct tunneling current during retention are necessary. However, the large magnitude of the P/E voltages required to achieve the substantial field asymmetry will lead to increased power consumption and short cycling endurance. Metal NC memories, in particular, can potentially push further voltage scaling due to large density of states, inherent field enhancement, selectable work function, and tunneling asymmetry between P/E and retention [3-4]. In addition, field-sensitive barrier engineering is another method to enhance the $t_R$ / $t_{PE}$ [4-6]. Previously, we reported a novel gate structure with $C_{60}$-embedded resonant tunneling barrier (RTB) [1]. The monodispersion nature of $C_{60}$ makes it a better choice than ultra-small Si NCs [5], which are prone to parametrical variation from non-uniformity in NC size and density. During P/E operations, carriers can resonant-tunnel through the orbital energies of $C_{60}$ at high electric fields, increasing the gate current significantly. However, misalignment of energy levels at low-bias conditions due to the HOMO-LUMO gap and large charging energy of $C_{60}$ renders long retention. The field-sensitive asymmetry results in improved $t_R$ / $t_{PE}$ ratio.

Molecular memories offer several distinct advantages. Large-area and cheap-processing methods such as spin-coating [7], ink-jet printing [8] or solution based self-assembly process [9-12] have been demonstrated on plastic, glass, or inorganic substrates. Also, the molecular properties can be tailored with the choice of chemistry for possible layer-by-layer (LBL) integration with improved CMOS compatibility [13]. However, integration and performance optimization are still hindered by several factors. First, the carrier transport mechanism is not well characterized due to large global defect density within the substrate, dielectric barrier, and interface. Second, molecules generally cannot withstand high temperature processing and has poor long-term reliability under electrical stress.

To address these issues, we investigate barriers with thermally and electrically stable molecules embedded in a well-studied Flash memory gate structure. Previously, we have reported three programmable molecular orbitals of 5-(4-Carboxyphenyl)-10, 15, 20-triphenyl-porphyrin-Co(II) (CoP) for multi-level storage [12]. Following the designs with $C_{60}$ [1], in this paper we embedded CoP as the RTB structure to achieve low voltage operation, efficient program/erase, and long cycling lifetime. CoP can form a self-assembled monolayer with approximately ten times the density of $C_{60}$, potentially leading to larger memory window or better P/E efficiency under identical programming conditions. In separate splits towards the all-organic dielectrics, the conventional oxide-based dielectric is replaced with a thermally stable, densely packed alkly chain with double functional groups, 16-Phosphonohexadecanoic acid (97%) (PHDA), for molecular LBL integration, which can potentially create large area, electrically robust molecular junctions and insulation. More importantly, a thorough understanding of the charge storage, dielectric and interface properties of molecular layers in a field-effect gate structure will pave the way for the design and fabrication of all-organic substrates, which offer a broad range of applications in large-area energy, displays and sensors.

## *4.3 Device Fabrication*

The design of experiments of MOS gate stack structures is shown in Figure 4-1. Figure 4-2 presents the molecular structure of CoP-COOH, CoP-$NH_2$, and PHDA. The detailed splits are summarized in Table 4-1. For memory cell structures (C, D, E and F), spherical Au NCs were self-assembled on oxide by electron-beam evaporation of 1.2 nm Au wetting layer without annealing. Then, 30nm $Al_2O_3$ was deposited by thermal atomic layer deposition (ALD) at 300 °C as control dielectric. Finally, a top

Al gate was deposited and patterned by photolithography, followed by 350°C forming gas annealing for 30 minutes. Cr/Au gate metals are evaporated through a shadow mask for process splits that involve LBL deposition to avoid contamination.

### 4.3.1. Hybrid Tunnel Barrier (HTB)

After standard RCA clean and a 15-second dip in diluted HF (1:20) to remove the native oxide of the p-type Si wafer (100), 2 nm rapid thermal $SiO_2$ followed by 3 nm ALD $Al_2O_3$ was grown to form the composite barrier. For high-quality, high-density CoP deposition, the wafer was immersed in a 1 mM CoP-COOH solution by dimethylformamide (DMF) / ethanol (1:1) at room temperature for 12 hours. After thorough rinsing with DMF, ethanol, and dichloromethane (DCM), the wafers were purged in nitrogen gas. Then, 3 nm of $SiO_2$ was grown by E-beam evaporation as the encapsulation layer.

### 4.3.2. Hybrid Tunnel Barrier (HTB) with Layer-by-Layer (LBL) integration

After standard RCA clean and a 15-second dip in diluted HF (1:20) to remove the native oxide of the p-type Si wafer (100), 1 nm of thermal ALD $Al_2O_3$ was grown as the attachment layer at 300°C. It should be noted that native oxide grows readily during the growth of ALD $Al_2O_3$ [12]. We verified that $Al_2O_3$ was grown on a thin layer of native oxide (~ 1 nm) with ellipsometry. Then, the wafer is immersed in a 5 mM PHDA solution of isopropanol (IPA) at room temperature for 24 hours to initiate the growth of PHDA on $Al_2O_3$ as the organic insulator. 1mM of N,N'-Dicyclohexylcarbodiimide (DCC) was added to the solution as a condensing agent. After thorough rinsing with IPA to remove undesired physically absorbed PHDA molecules, the wafer was immersed in a 1 mM CoP-$NH_2$ solution of DMF/ethanol (4:1) at 110°C for 2 hours. Due to the lower affinity of the carboxylic acid to $Al_2O_3$ in comparison with the phosphonic acid [14], adsorbed PHDAs are expected to have an orientation with the carboxyl groups floating on top, which can react with the amine

group of CoP-$NH_2$ to form an amide bond. After thorough rinsing with DMF, ethanol, and DCM, the wafers were purged in nitrogen gas. Subsequently, 3 nm of thermal ALD $Al_2O_3$ was grown at 110°C as the encapsulation layer.

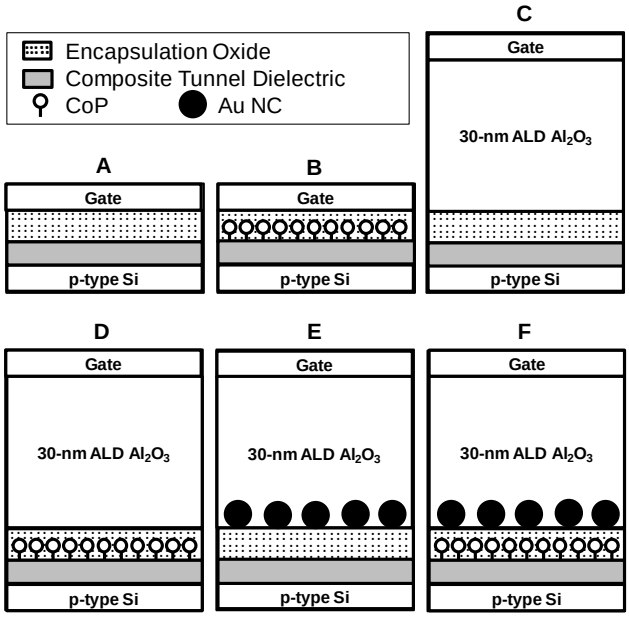
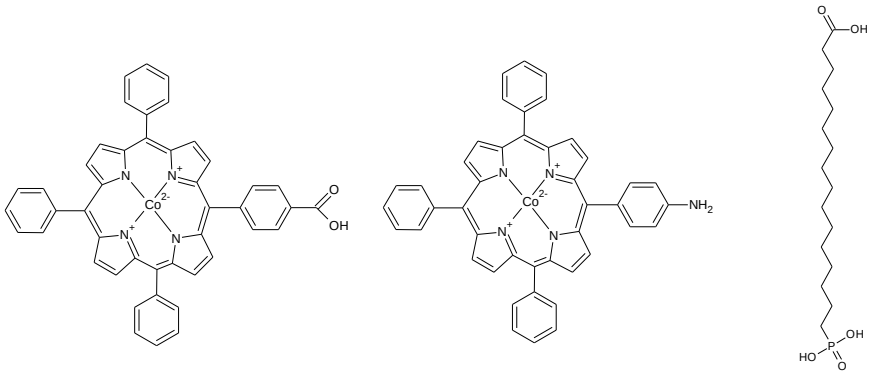



Figure 4-1 Schematics of the heterogeneous gate stacks examined in this work. The hybrid tunnel barrier (HTB) has a composite tunnel barrier (CTB) of 2 nm $SiO_2$ + 3 nm $Al_2O_3$ and an encapsulation oxide of 3 nm evaporated $SiO_2$. The HTB device with LBL integration has a CTB of 1 nm $SiO_2$ + 1 nm $Al_2O_3$ + PHDA and an encapsulation oxide of 3 nm thermal ALD $Al_2O_3$.




(a) (b) (c)

Figure 4-2 Molecular structures of (a) CoP-COOH, (b) CoP-$NH_2$, and (c) PHDA.

| Device | Composite Tunnel Barrier | CoP | Encapsulation Oxide | Au NC | Control Oxide | Gate |
|---|---|---|---|---|---|---|
| A1 | 2 nm $SiO_2$ + 3 nm $Al_2O_3$ | | 3 nm Evaporated $SiO_2$ | | | Al |
| A2 | 1 nm $SiO_2$ + 1 nm $Al_2O_3$ + PHDA | | 3 nm ALD $Al_2O_3$ | | | Cr/Au |
| B1 | 2 nm $SiO_2$ + 3 nm $Al_2O_3$ | o | 3 nm Evaporated $SiO_2$ | | | Al |
| B2 | 1 nm $SiO_2$ + 1 nm $Al_2O_3$ + PHDA | o | 3 nm ALD $Al_2O_3$ | | | Cr/Au |
| C1 | 2 nm $SiO_2$ + 3 nm $Al_2O_3$ | | 3 nm Evaporated $SiO_2$ | | 30 nm ALD $Al_2O_3$ | Al |
| C2 | 1 nm $SiO_2$ + 1 nm $Al_2O_3$ + PHDA | | 3 nm ALD $Al_2O_3$ | | 30 nm ALD $Al_2O_3$ | Cr/Au |
| D2 | 1 nm $SiO_2$ + 1 nm $Al_2O_3$ + PHDA | o | 3 nm ALD $Al_2O_3$ | | 30 nm ALD $Al_2O_3$ | Cr/Au |
| E1 | 2 nm $SiO_2$ + 3 nm $Al_2O_3$ | | 3 nm Evaporated $SiO_2$ | o | 30 nm ALD $Al_2O_3$ | Al |
| E2 | 1 nm $SiO_2$ + 1 nm $Al_2O_3$ + PHDA | | 3 nm ALD $Al_2O_3$ | o | 30 nm ALD $Al_2O_3$ | Cr/Au |
| F1 | 2 nm $SiO_2$ + 3 nm $Al_2O_3$ | o | 3 nm Evaporated $SiO_2$ | o | 30 nm ALD $Al_2O_3$ | Al |
| F2 | 1 nm $SiO_2$ + 1 nm $Al_2O_3$ + PHDA | o | 3 nm ALD $Al_2O_3$ | o | 30 nm ALD $Al_2O_3$ | Cr/Au |
| $C_{60}$-RTB [1] | 2.5 nm $SiO_2$ | | 3 nm Evaporated $SiO_2$ | o | 30 nm PECVD $SiO_2$ | Cr |

Table 4-1 Design of experiments of RTB and RTB-based memory cell structures.

## *4.4 Results and Discussion*

### 4.4.1. Surface Characterization and Thermal Stability Analysis

From the X-ray photoelectron spectroscopy (XPS) in Figure 4-3, distinct peaks of the $2p_{1/2}$ and $2p_{3/2}$ electron configuration corresponding to the orbital binding energies of cobalt and phosphorous can be clearly observed for the CoP and PHDA SAMs, respectively. The characteristic peaks are evidence of CoP-COOH and PHDA deposited on $Al_2O_3$ and CoP-$NH_2$ adsorption on PHDA. The XPS features may also be used to estimate the surface densities of the SAMs [12, 15], where we used XP spectra from the evaporated Au (not shown) on is used as a reference standard. The details of the quantization method are explained in previous reports [12, 15]. Assuming the molecules form a finite thickness on the surface, $d_{SAM}$, with atomic density $N_{SAM}$, and $d_{SAM}$ << inelastic mean free path of SAM, $\lambda_{SAM}$, the surface density, $D_{SAM} = N_{SAM} d_{SAM}$ (molecules/cm$^2$), of CoP-COOH, CoP-$NH_2$, and PHDA can then be calculated to be $3.6 \times 10^{13}$, $5.84 \times 10^{13}$, and $1.8 \times 10^{14}$ molecules/cm$^2$, respectively. $\lambda$ is experimentally determined by measuring the photoelectron intensity as a function of the layer thickness. Considering the assumptions behind the estimation and the background noise, the absolute accuracy is approximately ±35%.

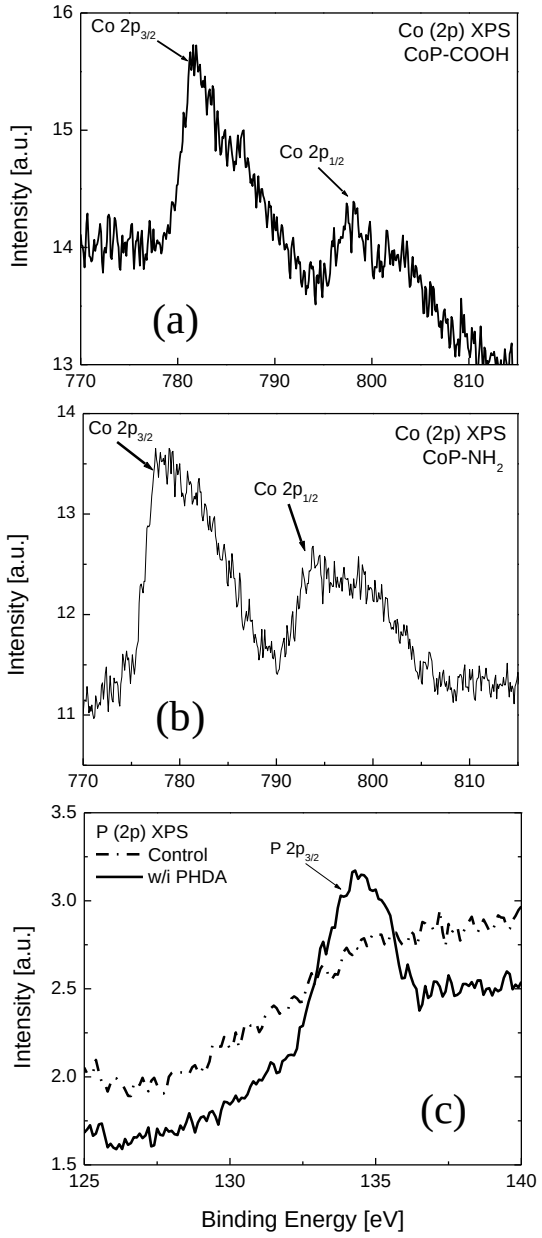



Figure 4-3 X-ray photoelectron spectroscopy (XPS) data of (a) CoP-COOH SAM deposited on thermal ALD $Al_2O_3$, (b) CoP-$NH_2$ SAM deposited on PHDA, and (c) PHDA deposited on thermal ALD $Al_2O_3$. Sample (a) and (b) were rinsed with pure DMF/ethanol (4:1) and dichloromethane (DCM) for three rounds each, in sequential order, before taking the XPS spectra. Sample (c) was rinsed with three rounds of pure IPA before taking the XPS spectra.

The surface densities of the CoP layers are in close agreement with previous estimates by cyclic voltammetry (CyV) [9], whereas the PHDA density is slightly sparser than expected. To understand this, the surface density of an alkyl chain with similar molecular structure as PHDA, but with a $-CH_3$ instead of carboxyl terminal group, has been estimated to be $4.4 \times 10^{14}$ $cm^{-2}$ by XPS. Therefore, we believe the repulsion force from negative charged carboxyl group may have attributed to the sparser density of PHDA or smaller average $d_{SAM}$.

To examine the thermal budget of the molecular layers, we performed thermogravimetric analysis (TGA) on CoP-COOH and PHDA in Figure 4-4. CoP-$NH_2$ is expected to have nearly identical thermal budget as CoP-COOH since the functional group attributes only to a small portion of the overall molecular mass. No significant weight loss was observed below 400°C for either molecule. The superior thermal stability agrees well with previous reports [18-19].

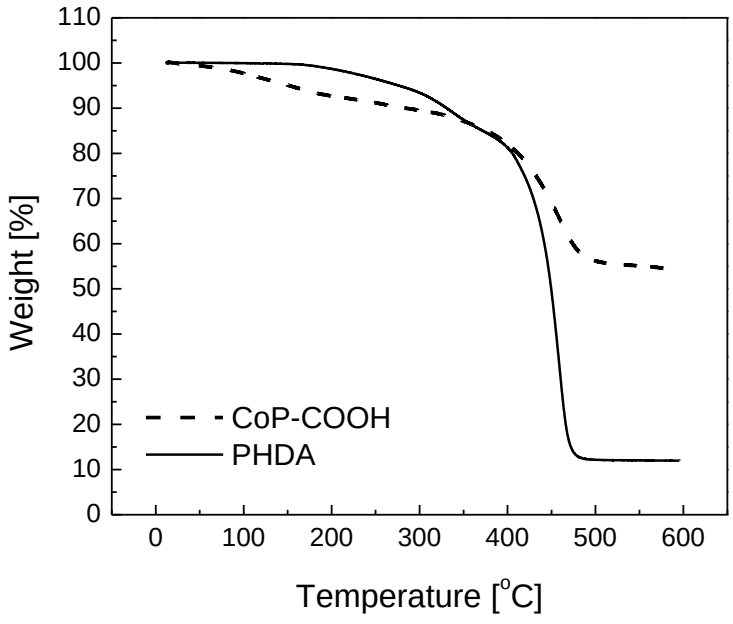



Figure 4-4 Thermogravimetric analysis (TGA) data of CoP-COOH and PHDA.

### 4.4.2. Gate Current of Resonant Tunneling Barrier

As discussed earlier, at high electric fields, carriers with enough energy to overcome the Coulomb blockade and quantum confinement energies can resonant-tunnel through the molecular energy levels of a small-bandgap redox-active molecule, such as $C_{60}$ or CoP, sandwiched between two large-bandgap insulators. Depending on the energy alignment, at low electric fields, the direct tunneling current through the thick composite barrier can be very small. To observe the resonant tunneling effect, we first examine the gate current and high-frequency-capacitance-voltage (HFCV) characteristics of the tunnel barrier structures in Figure 4-5. B1 and B2 are CoP-embedded RTB structures. A1 and A2 are control samples without the CoP layers.

***J-V of Hybrid Tunnel Barrier (RTB)***

From the CV characteristics, the effective oxide thickness (EOT) of the tunnel barrier is thicker with the CoP layer (B1) than without the CoP layer (A1). The CoP layer thickness measured by ellipsometry agrees with the EOT extracted from the oxide capacitance. Despite thicker EOT, the gate current density with the CoP-embedded tunneling barrier increases by ~ 3 orders of magnitude. As illustrated in Figure 4-6, all tunnel barriers show weak temperature dependence, suggesting elastic tunneling process as the dominant transport mechanism. Among all tunnel barrier structures, only A1 shows a small increase in current density with increasing temperature. In section *E*, the P/E transients of the memory structures will be compared to confirm the temperature effect on carrier storage. It is however difficult to directly observe the signature negative-differential-resistance (NDR) representing resonant tunneling due to Coulomb force disturbance from neighbor molecules [12] and non-uniform thickness of the encapsulation oxide.

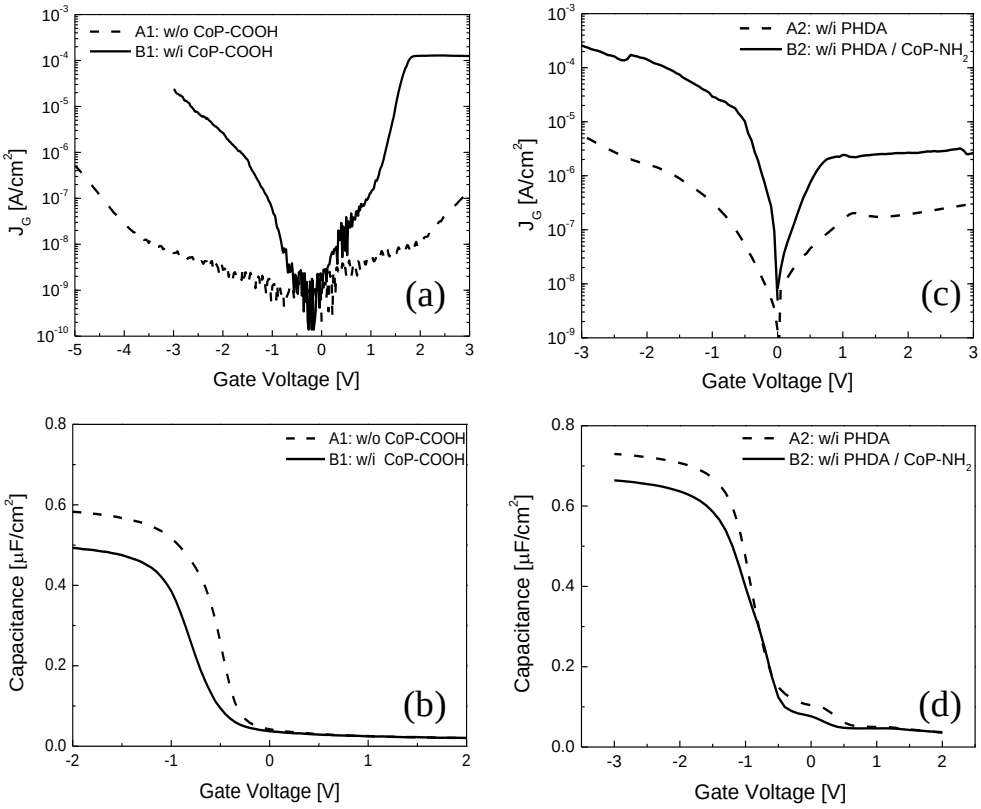



Figure 4-5 Gate current and high frequency CV (HFCV) measurements of A1, A2, B1, and B2. B1 consists 2 nm $SiO_2$ + 3 nm $Al_2O_3$ + CoP-COOH + 3 nm evaporated $SiO_2$. B2 consists 1 nm $SiO_2$ + 1 nm $Al_2O_3$ + PHDA + CoP-$NH_2$ + 3 nm thermal ALD $Al_2O_3$. A1 and A2 are the corresponding control samples without the functionalized CoP molecules.

***J-V of PHDA molecules with Layer by Layer (LBL) Deposition***

As illustrated in Figure 4-5(c), despite of thicker EOT, the CoP-embedded structure (B2) with LBL deposition also demonstrates more than an order of magnitude increase in gate current density compared to the structure without the CoP layer (A2). The extracted EOT of the CoP layer is less than the estimated thickness by ellipsometry, possibly due to the encapsulation high-$\kappa$ $Al_2O_3$ surrounding the CoP molecules. As illustrated in Figure 4-6, the relatively weak temperature dependence of

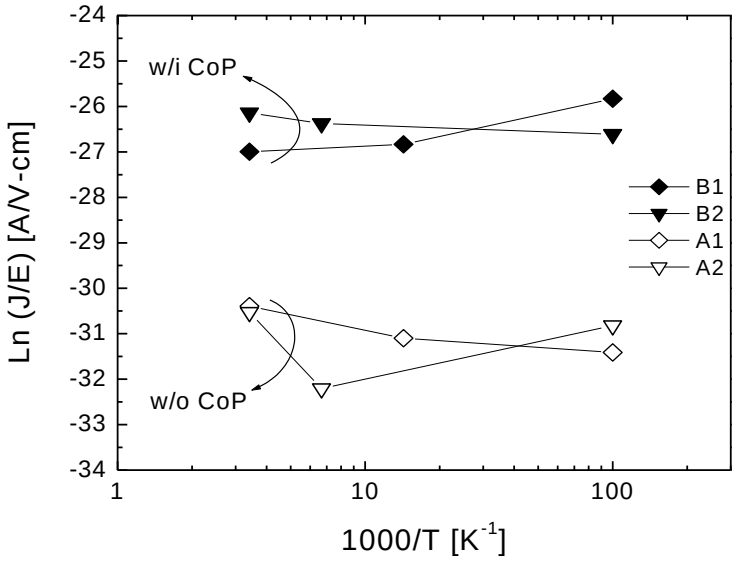



Figure 4-6 (a) *J-E* characteristics of all tunnel barrier structures and (b) *J-V* characteristics of A2 at various temperatures. For (a), the electric field is fixed at – 4.3 MV/cm for A2, B1, and B2. The electric field is set at – 8.3 MV/cm for A1 due to the smaller signal to noise ratio at lower fields.

A2 with just the LBL PHDA gate stack is in contrast with previous reports on organic alkyl SAM and ALD $Al_2O_3$, where the *J-V* characteristics usually fit the Frenkel-Poole (F-P) model [20-21]. We believe the improved interface quality can be attributed to the LBL deposition method, leading to less pronounced F-P conduction. To study the reliability under high-field stress, Figure 4-7(a) illustrates the breakdown (BD) characteristics of A2, B2, and the control sample without any organic layers. Introducing PHDA suppresses the gate current by ~ 3 orders of magnitude, but the BD voltage is only moderately improved, perhaps resulting from the incomplete surface coverage of PHDA that encourages filament growth. Figure 4-7(b) shows the *J-V* characteristics under constant current stress (CCS) of $J$ = 1 mA/cm$^2$, applied up to a total fluence of 1 C/cm$^2$. The control sample shows negligible charge trapping or trap

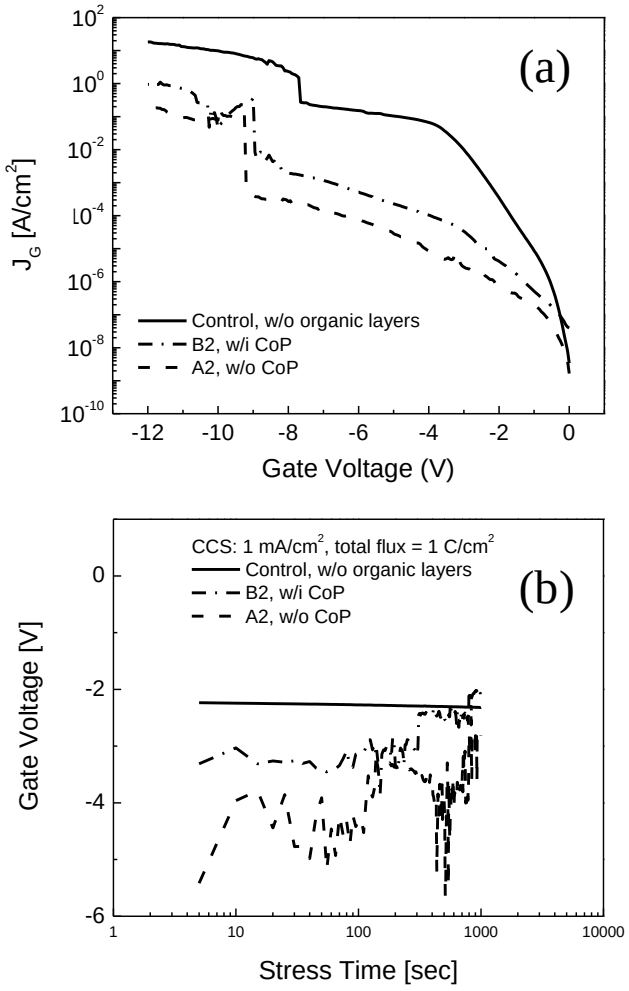



Figure 4-7 (a) Breakdown characteristics and (b) constant current stress results of A2, B2, and the control device without any organic layers.

generation behavior, whereas both A2 and B2 show gradual increase in gate current, indicating generation of new traps. For A2, the current oscillation behavior over time suggests carriers being captured and released from the trap sites. Although the carboxyl group can readily form covalent bonds with the TMA precursor of thermal ALD $Al_2O_3$, dangling bonds may form between PHDA molecules as a result of the incomplete surface coverage. B2, on the other hand, shows less charge trapping behavior because carriers were transported through the orbital states of CoP, which

has a higher and more controllable density than the interface states, instead of relaxing to nearby trap sites. Since the carrier transport efficiency is improved, B2 also shows less stress-induced-leakage-current (SILC) under the same fluence.

### 4.4.3. Improved Tunneling Asymmetry in Flash Memory with Resonant Tunneling Barrier

***Hybrid Tunnel Barrier (HTB)***

Flatband voltage shift ($\Delta V_{FB}$) as a function of the gate voltage is shown in Figure 4-8(a) for HTB memory cells without (E1) and with the CoP layer (F1).

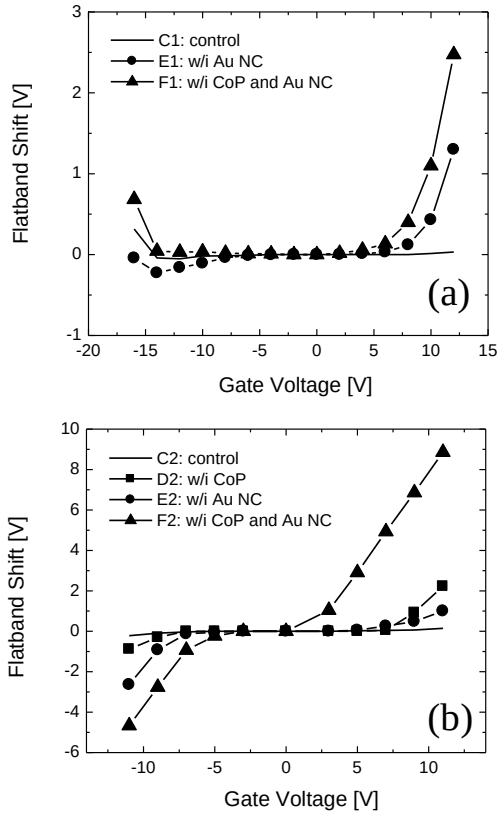



Figure 4-8 Flatband voltage shift as a function of the gate voltage for memory cells with (a) HTB (C1, E1, F1) and (b) HTB with LBL integration (C2, D2, E2, F2). In (a), electron carrier injection efficiency is improved with resonant tunneling nodes of CoP. In (b), both electron and holes are injected more efficiently with the CoP layer.

Both devices have the Au-NC charge storage layer. For a control sample without either Au NC or CoP (C1), negligible $\Delta V_{FB}$ was observed under identical bias conditions. In F1, much larger positive $\Delta V_{FB}$ indicate preferable electron storage by resonant tunneling, whereas hole storage is less preferable within the bias range. The preference for electron storage was previously explained by the Fermi-level pinning theory [22]. The charge neutrality level (CNL) can be regarded as a local Fermi-level of the interface states, which are dangling bonds that disperse across the band gap of the dielectric. The CNL of $Al_2O_3$ deposited by ALD is around –5.2 eV [23], which gives an effective Au work function even deeper than –4.9 eV, suppressing hole storage to the Au NCs. To illustrate the improved tunneling asymmetry by $t_R$ / $t_{PE}$, we first examine the retention and P/E characteristics of the full Flash memory cell in Figure 4-9. Compared to ~ 3 orders increase in gate current shown in Fig. 3(a), the P/E efficiency of F1 improves by about one order of magnitude, which may be the result of current saturation due to substrate resistance or insufficient minority carrier generation under higher electric fields. In addition, P/E time of E1 is noticeably longer at 10 Kelvin, whereas F1 shows relatively small temperature dependence. This confirms our previous argument that elastic tunneling process is the dominant transport mechanism for the CoP-embedded tunneling barrier, as illustrated from the temperature-independent *J-E* characteristics in Figure 4-6, whereas A1 (without the CoP layer) shows slightly stronger temperature dependence. Programming efficiency improves further at longer pulses as resonant tunneling to upper Au NC begins to dominate. Both E1 and F1 show excellent retention characteristics at room temperature due to the thick physical barrier and deep Fermi energy of Au NC. At 90°C, F1 shows improved electron retention compared to E1 due to the CoP HOMO-LUMO gap, which suppresses tunneling back to the substrate [1].

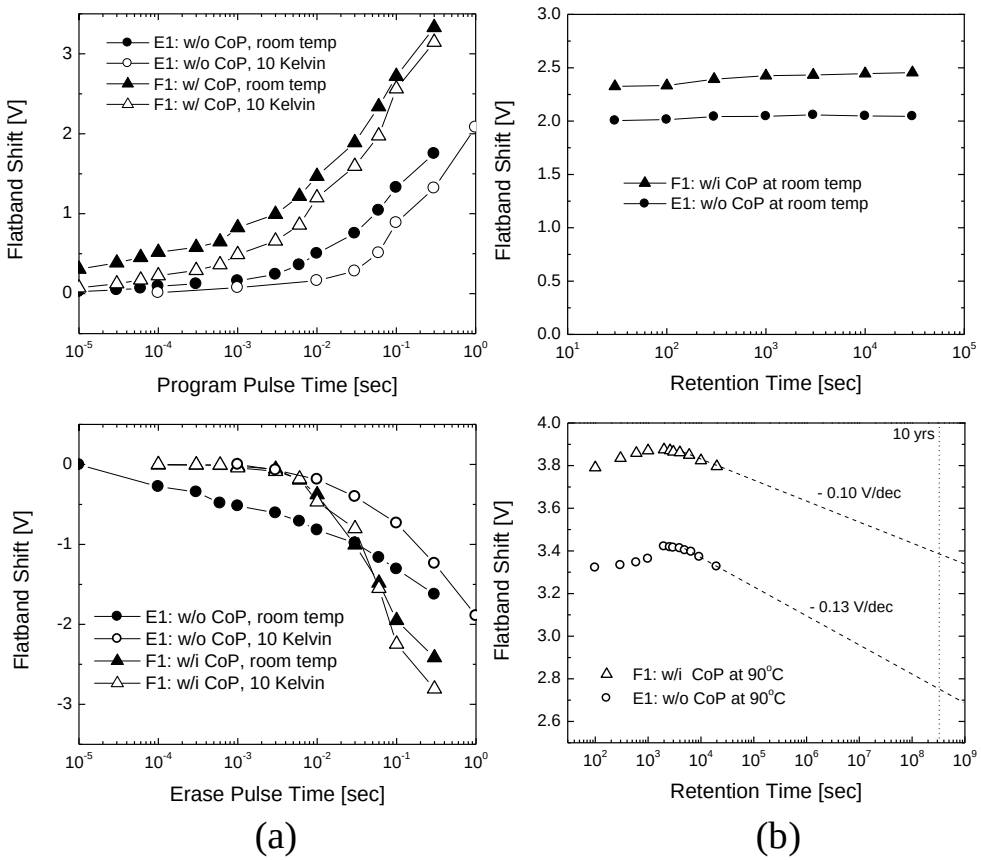



Figure 4-9 (a) P/E transients and (b) charge retention of memory cells with HTB (E1 and F1). The P/E voltages were set at ±16 V. P/E tests were performed both at room-temperature and at 10 Kelvin to determine whether carrier transport is elastic. Devices were programmed prior to the erase measurements. A controlled light source was shed on the devices to promote minority carrier generation for electron programming measurements.

***PHDA Molecules with Layer by Layer (LBL) Deposition***

In Figure 4-8(b), $\Delta V_{FB}$ as a function of the programming voltage is shown for HTB memory cells with LBL deposition of PHDA and CoP molecules. Without the presence of organic layers (C2), negligible $\Delta V_{FB}$ was observed within the bias range. Consistent with the measurements on F1, electron injection is preferred with CoP (D2, F2). The memory cell with PHDA, but without CoP (E2) shows preference for hole

storage, which is consistent with previous measurements on the HTB structure without the CoP (E1) layer. It may be worth noting that E1 prefers electron injection, whereas E2 has a preference for hole injection, owing to the difference in metal work function. E2, which has a Cr/Au gate instead of Al, has a deeper gate work function, preventing gate injection through the leaky control dielectric at negative bias. Therefore, despite the large tunneling current shown in Figure 4-5(a), the erase efficiency of devices with an Al gate is severely compromised, likely due to gate injection. Similar observations have been reported previously [24-25]. With both CoP and Au NC (F2), the nearly symmetric increase in $\Delta V_{FB}$ indicates improved injection efficiency through the resonant-tunnel modes of CoP to the Au NCs for both electrons and holes.

In Figure 4-10, the memory cell with LBL deposition shows similar improvement in tunneling asymmetry with HTB. However, the P/E measurements were initiated from a flatband condition to avoid complications involving the injected charge that has relatively poor retention, which will be discussed later. At ±10 V, both electron and hole injection efficiencies of F2 (with CoP-$NH_2$) are at least 20 times faster than E2 (without CoP-$NH_2$), in qualitative agreement with the *J-V* characteristics. At ±16 V, electron injection efficiency becomes nearly 100 times faster with CoP, whereas hole injection efficiency improves moderately. It should be noted that the programming speed of E2 improved by at least 3 orders of magnitude as we increase the gate voltage from +10 to +16 V. The sharp increase in electron injection efficiency under higher electric field offers an indirect evidence of resonant tunneling through the CoP orbital energies. Under lower electric fields, resonant tunneling is suppressed by the molecular energy gap and Coulomb blockade energies.

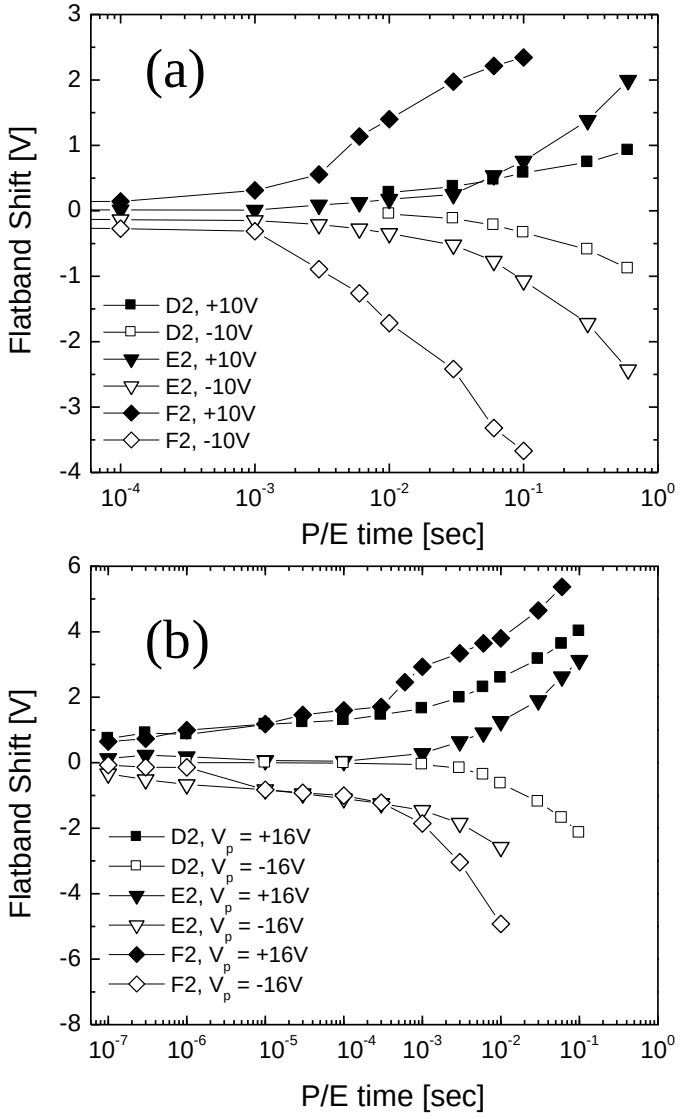



Figure 4-10 P/E transients of memory cells with LBL integration (D2, E2, and F2) at (a) ± 10 V and (b) ±16 V. To avoid complications involving poor carrier retention, P/E measurements were initiated from a flatband condition. A controlled light source was shed on the devices to promote minority carrier generation for electron programming measurements.

Figure 4-11 examines the P/E pulse time as a function of the gate bias of F2.

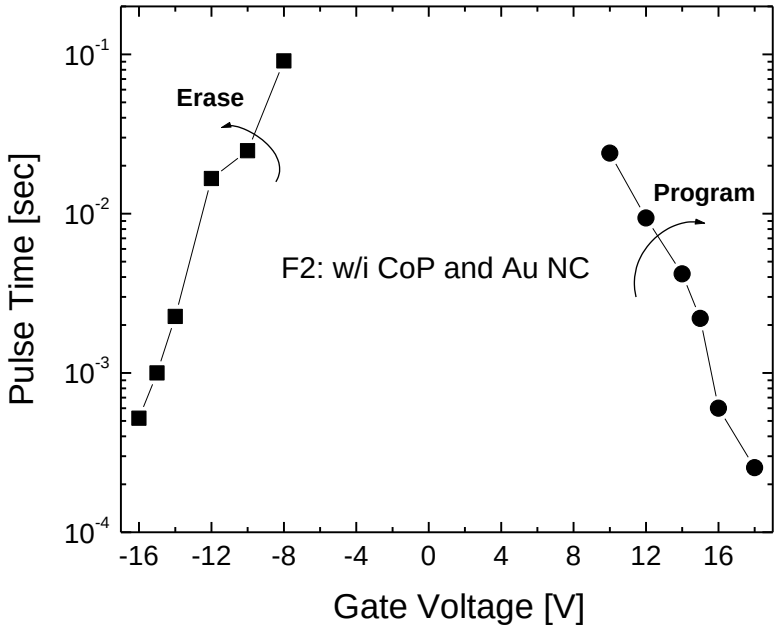



Figure 4-11 P/E characteristics as a function of P/E voltage for F2 (with both CoP and Au NC). The program and erase states are set at $V_{FB}$ = 3 and –1 V, respectively. A controlled light source was shed on the devices to promote minority carrier generation for electron programming measurements.

The pulse time decreases at a moderate rate with increasing gate bias, which agrees with the trend observed in the *J-V* characteristics of B2. In addition to the improved P/E efficiency, CoP-embedded cells show ~ 2 orders of magnitude improvement in retention time for both electron and holes, as illustrated in Figure 4-12. As discussed earlier, the Coulomb blockade and HOMO-LUMO gap of CoP may have suppressed trap-assisted tunneling back to the substrate. Electron retention is however severely compromised with LBL deposition in comparison with HTB. We attribute this difference to the encapsulation oxide. As oppose to the deep CNL of ALD $Al_2O_3$, the CNL of evaporated $SiO_2$ is likely near the silicon conduction band [1], creating a

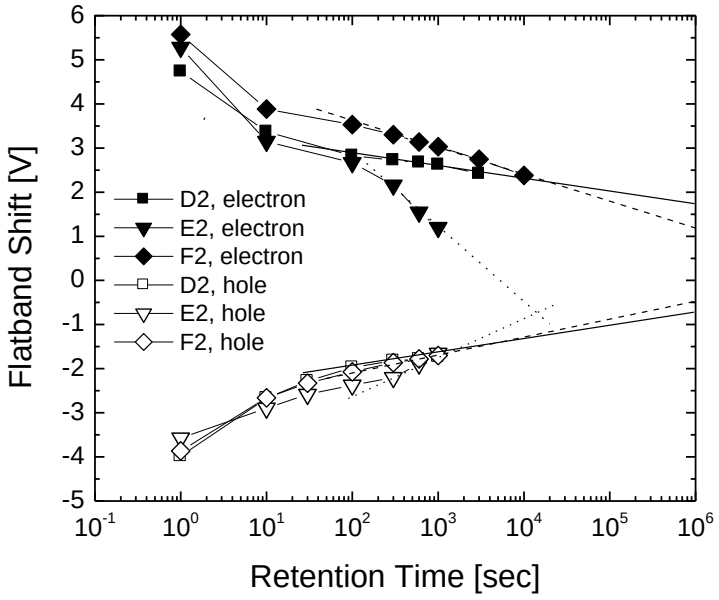



Figure 4-12 Room-temperature retention characteristics of memory cells with LBL integration (D2, E2, and F2).

higher barrier for carriers to leak back to the substrate. Finally, the endurance characteristics of D2, E2, and F2, are compared in Figure 4-13. The P/E conditions were chosen to achieve comparable memory window. The programming condition is set at +16 V for 10 ms. For D2 and E2, the erase conditions are –16V for 30 ms and 2 ms, respectively. F2 was erased at –10 V for 50 ms. F2 shows negligible memory window loss up to $10^4$ P/E cycles, whereas D2 and E2 retain approximately 70% and 80% of memory window after 1000 P/E cycles, respectively. Under similar voltage stress, E2 has a slightly better endurance over D2, which agrees with the breakdown characteristics of the tunnel barrier structure in Figure 4-7(a). B2 has a slightly smaller breakdown voltage due to dangling bonds at the CoP/$Al_2O_3$ interface, which leads to additional trap sites contributing to the formation of percolation paths. In contrast, F2 benefits from both resonant tunneling through the energy levels of CoP and larger

capture cross-section of Au NC, which further enhance carrier transport. For the same memory window, lower P/E voltages put less stress on the tunnel barrier leading to longer cycling endurance.

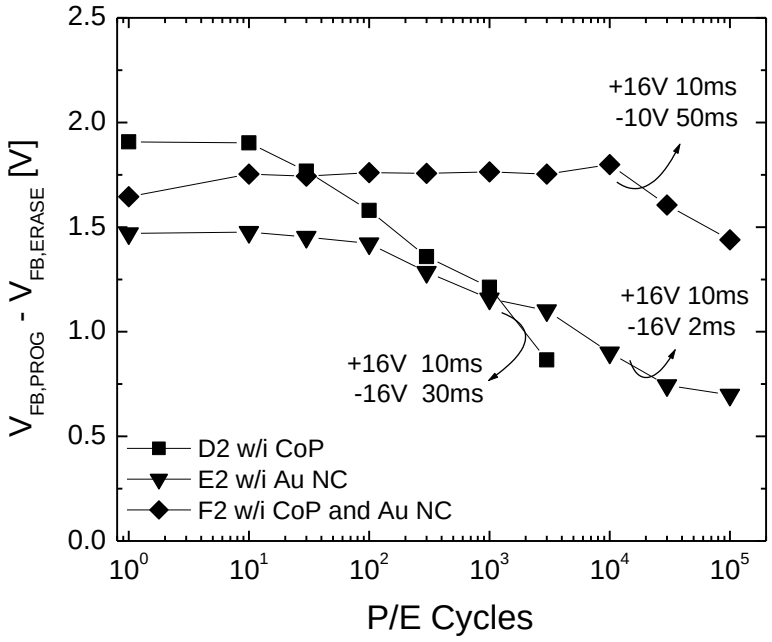



Figure 4-13 Endurance characteristics of memory cells with LBL integration (D2, E2, and F2). The P/E conditions for each structure are shown. A controlled light source was shed on the devices to promote minority carrier generation during the cycling measurements.

| Device | Tunnel Barrier EOT (nm) | $e^-$ $t_R$ / $t_P$ increase (orders) | $h^+$ $t_R$ / $t_P$ increase (orders) |
|---|---|---|---|
| F1 (HRTB) | 6.99 | 6 | N/A |
| F2 (HTB w/ LBL) | 5.19 | 2.5 | 2 |
| $C_{60}$-RTB [1] | 5.5 | 1 | -1 |

Table 4-2 $t_R$ / $t_{PE}$ improvement of Au NC memory cell with various molecular-embedded RTB structures. $t_R$ is defined at 50% charge loss from the extrapolated retention time. $t_{PE}$ is defined at the time when $|\Delta V_{FB}|$ = 0.2 V. Negligible hole storage was observed for F1.

## *4.5 Conclusion*

To benchmark performance, the approximate $t_R$ / $t_{PE}$ improvements with or without the resonant-tunnel nodes are summarized in Table 4-2. Compared to $C_{60}$-embedded RTB, HTB with LBL deposition demonstrates $t_R$ / $t_{PE}$ improvement for both carrier types. Further optimization would be possible by integrating a redox-active molecule with multiple carboxyl groups to form covalent bonding with the trimethylaluminum (TMA) precursor of thermal ALD $Al_2O_3$, which may alleviate the Fermi-level pinning effect.

We have successfully demonstrated improved RTB-based injection from the *J-V* characteristics and enhanced $t_R$ / $t_{PE}$ ratio of CoP-embedded Au-NC memory cells. With the LBL deposition method, the improved $t_R$ / $t_{PE}$ for both carrier types may allow integration with both n-type or p-type organic semiconductors. Improved tunneling efficiency also puts less stress on the tunnel dielectric, leading to longer cycling lifetime. The solution-based molecular deposition is a simple and cost-effective method for creating large area molecular junctions. In addition, LBL integration may lead to fewer defect states at the dielectric interface, and better immunity to SILC without the need for high-temperature annealing.

### 4.5.1. Reflection

To eliminate interfacial traps at the molecular/dielectric interface, we attempted an ozone treatment to convert the vinyl tail groups of redox-active protoporphyrins (PP) into carboxyl groups. Following a previous demonstration with alkyl SAM [26], the carboxyl groups of PP can potentially form covalent bonds with the TMA precursor of ALD $Al_2O_3$. However, the ozone etches PP even at diluted concentration (1ppm/min). The concept is still worth another look with alkyl SAM. If integrated successfully, we can potentially achieve higher surface coverage and suppress the leakage current, which led to the poor retention for devices with LBL deposition.

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# CHAPTER 5

# INTERFACE AND OXIDE QUALITY OF CoFeB/MgO/Si TUNNEL JUNCTIONS

## *5.1 Abstract*

CoFeB/MgO/Si MOS capacitors were characterized to study the oxide and interface quality of very thin MgO layer (< 2 nm) after various annealing conditions. The improvement in tunneling magneto-resistance (TMR) ratio of a CoFeB/MgO/CoFeB composite layer is believed to result from Boron (B) diffusion into the MgO layer to form a polycrystalline Mg-B-O layer, which has a much sharper interface after annealing. By studying the stress-induced-leakage current (SILC) and the current oscillation component of the MOS structures, we were able to monitor the trap density, interface quality and endurance of the dielectrics. With the CoFeB capping layer, the dielectric defect density is indeed smaller upon interface formation, which may have led to the increase in TMR. Thermal annealing results in a sharper interface and superior endurance quality with the capping layer, but the interface trap density is only marginally improved.

## *5.2 Introduction*

Magnetic tunnel junction (MTJ) has attracted great interest as a possible candidate for the next generation magnetic random access memory (MRAM). Instead of the conventional Al–O, theoretical predictions suggest that implementing MgO as the tunneling barrier can achieve extremely high TMR due to proper electrode alignment, which promotes coherent spin-filtered tunneling [1-2]. For practical device applications involving complicated multilayer structures, sputter deposition of MgO between CoFeB electrodes is preferred over molecular beam epitaxy (MBE). Recently, sputter grown CoFeB/MgO/CoFeB MTJ with TMR of 604% at 300K was achieved [3]. In addition, the superior thermal stability of MgO-based MTJ (> 400°C) is attractive for manufacturing Si-based spintronic devices. Studies have suggested that TMR is highly dependent on the post-annealing conditions [3-16]. The improvement in TMR is believed to result from B diffusion into the MgO interface to form an energetically favorable polycrystalline Mg-B-O layer with a shaper interface. For very thin MgO (< 2nm), a recent study argued that the formation of Mg-B-O is observed throughout the thickness of the barrier layer, and TMR increases from a modest 25% to about 200% after annealing at 350°C [4]. Compared to as-grown MgO, where pinholes and interfacial defects may be prevalent, formation of a sharper CoFeB/Mg-B-O interface can enhance coherent tunneling due to crystallization after annealing, leading to higher TMR [3-9]. However, other groups have claimed that B enrichment is detrimental to the performance of the MTJ with CoFeB electrodes [10]. This discrepancy is due to the fact that the crystallization process and the nature of magnetization change are still not fully understood with the subsequent annealing process. In this study, highly sensitive electrical characterization on the CoFeB/Mg-B-O quality is used to explain the increase of TMR and associated reliability to confirm the boron diffusion effect upon annealing [4-9]. The trap charge in the MTJ structure

will change the tunneling path and cause serious parametric drift, but it is difficult to measure directly in a metal-insulator-metal structure. Instead, we made CoFeB/MgO/Si MOS capacitors with the process flow illustrated in Figure 5-1, which can independently determine the interface traps, oxide charge and stress-induced leakage current (SILC) through current-voltage (IV) and high-frequency capacitance-voltage (HFCV) measurements. We then characterized the boron diffusion and annealing effects on Mg-B-O to provide a complementary study.

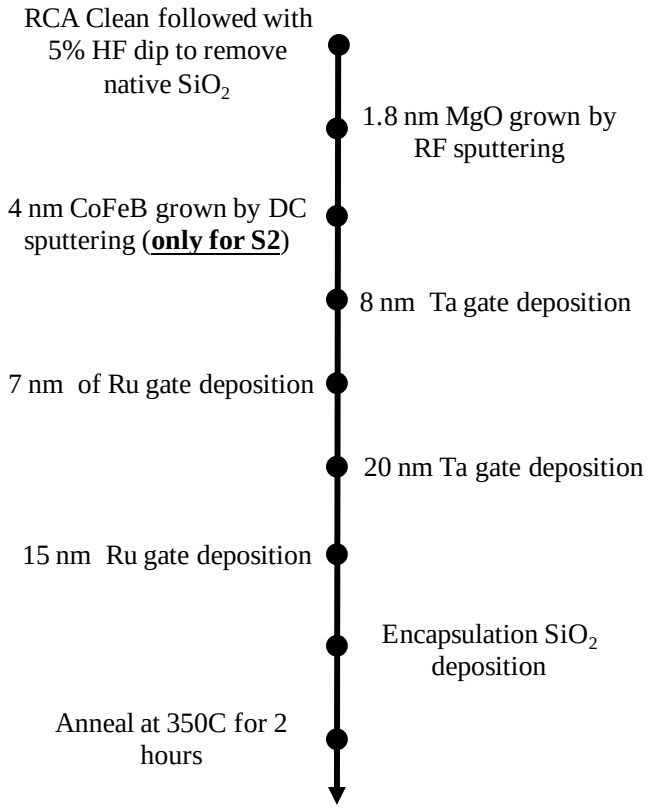



Figure 5-1 Process flow of the MTJ device. S1 is a control sample with identical process flow as S2, but without CoFeB deposition.

## *5.3 Device Fabrication*

Both DC and RF magnetron sputtering was used to grow all layers on p-type Si (100) substrates at a base pressure ~ $2\times 10^{-3}$ Torr with different resistivity (S1: 10 Ω/cm, S2: 0.1 Ω/cm). Two substrate dopings were chosen to compare the current quantum-oscillation component with different substrate resistance [20-21]. For S2, after standard RCA cleaning and a short 15-second dip in HF solution to remove the native oxide, 1.8 nm MgO followed by 4 nm CoFeB were grown. Thin layers of Ta (8 nm) and Ru (7 nm) were deposited first to block metal contamination followed by thicker layers (Ta: 20 nm, Ru: 15 nm) to avoid damage to the MTJ during contact. The sidewalls of the gate stacks were encapsulated by $SiO_2$ with a liftoff process to avoid ambient contamination. A control sample with identical layers, but without the CoFeB layer (S1) was fabricated to study the B diffusion effect. The process flow is illustrated in Fig. 1. Devices were studied as-grown and after 2 hours annealing at 350 °C under a base pressure of $5\times 10^{-6}$ Torr. The films were patterned into capacitor structures with size of $60\times 60\ \mu m^2$.

## *5.4 Results and Discussion*

With the presence of the CoFeB layer, previous studies have shown that for thin MgO (< 2nm), the RF sputtering process forms a Mg-B-O layer throughout the thickness of the barrier after deposition [4], and annealing further increases the intensity of $BO_x$ bonding, which has been confirmed by XPS [9, 11]. The HFCV measurements indicates improved oxide quality in terms of trap densities with the incorporation of B diffusion and annealing processes, as illustrated in Figure 5-2.

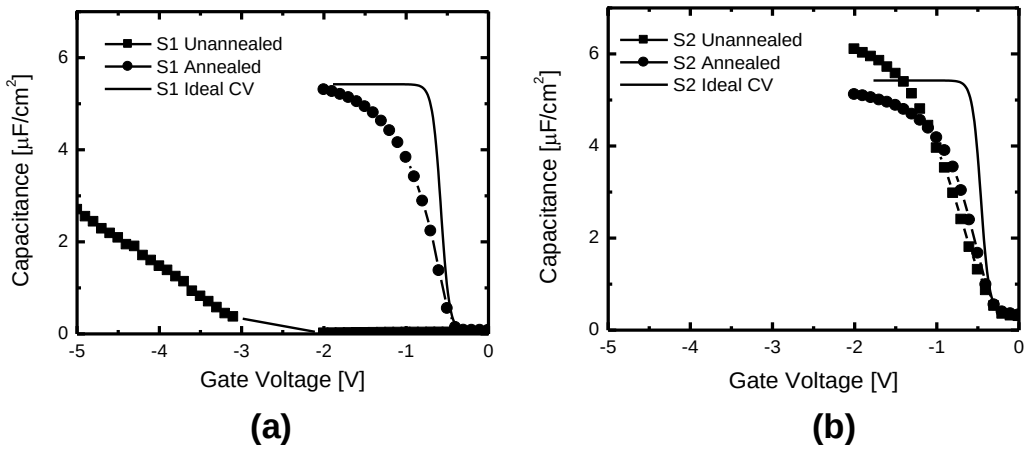



Figure 5-2 HFCV characteristics of as-grown and annealed (a) S1 and (b) S2.

Flatband voltage shift ($\Delta V_{FB}$) away from the ideal value and the "stretch out" behavior observed in S1 is usually attributed to fixed oxide charge and interfacial traps, respectively. Prior to annealing, the sharper transition slope and a $V_{FB}$ closer to the ideal value suggest that as-grown Mg-B-O in S2 forms a more ideal barrier with less defect sites compared to as-grown MgO. After annealing S1, the residual stress associated with sputtered MgO [7] is relaxed to form a smoother interface with Ta. Since CoFeB is an amorphous alloy, the residual stress of as-grown CoFeB/MgO interface would be less than Ta/MgO. Another possible explanation for the large stretch-out behavior observed in as-grown S1 may be attributed to the formation of a leaky $Ta_2O_5$ layer at the Ta/MgO interface during sputter deposition. It is interesting to note that the oxide capacitance of as-grown S2 does not saturate to the same value as annealed S2 due to oxide leakage current [17]. As illustrated in Figure 5-4(b), the gate current density is indeed lowered by approximately an order of magnitude after annealing. To quantify the B diffusion effect on dielectric quality,

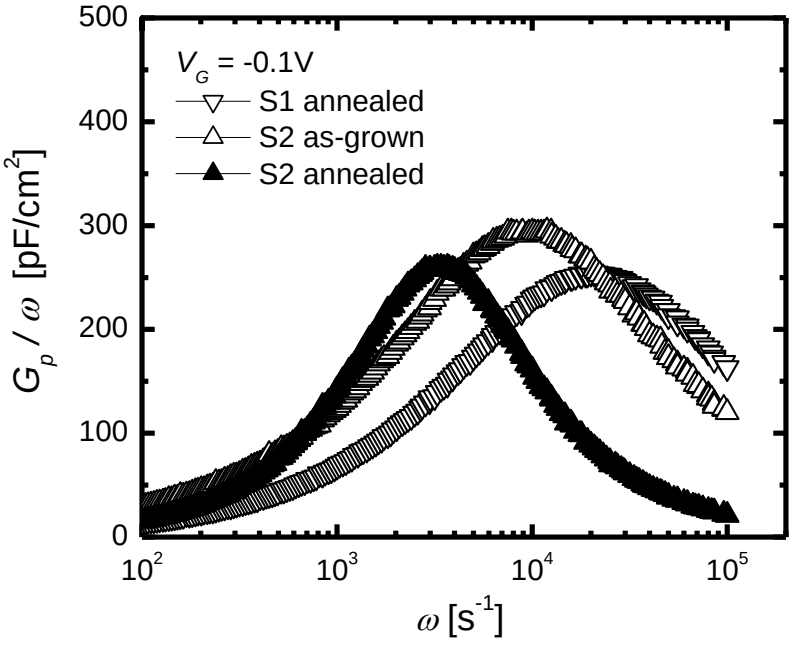
Figure 5-3 shows the capacitance loss, $G_p$ / $\omega$, versus frequency, $\omega$, and the corresponding interface trap density ($D_{it}$) estimated by the conductance method [17]. The conductance loss can be extracted from the following relation:

$$\frac{G_p}{\omega} = \frac{\omega C_{ox} G_m}{G_m{}^2 + \omega^2 (C_{ox} - C_m)^2} \qquad (1)$$

where $C_m$ is the measured capacitance, $C_{ox}$ is the measured capacitance in strong accumulation regime, $G_m$ is the measured conductance, and $G_p$ is the equivalent parallel conductance. With the peak value of $G_p$ / $\omega$, $D_{it}$ can be estimated with the following expression [18]:

$$D_{it} = \frac{2.5}{q}\left(\frac{G_p}{\omega}\right)_{\max} \qquad (2)$$

With or without the presence of CoFeB, the $D_{it}$ is high, which may be the result of lattice mismatch between the sputtered dielectric and the underlying Si [19]. After annealing S2, $D_{it}$ decreases only slightly. This agrees with the nearly identical CV transition slope. For as-grown S1, the measured admittance becomes frequency independent due to the large leakage between the gate and the trap states, prohibiting trap density estimation.




| | S1 (annealed) | S2 (as-grown) | S2 (annealed) |
|---|---|---|---|
| $D_{it}$ ($\times 10^{13}$ cm$^{-2}$) | 1.76 | 2.05 | 1.81 |

Figure 5-3 Capacitance loss, $G_p$ / $\omega$, as a function of frequency for as-grown S2 and annealed S1 and S2. The interface trap densities ($D_{it}$) are listed in the table.

As illustrated in Figure 5-4, for as-grown S1, the large $D_{it}$ attributed to the sharp increase in current density at very low voltages suggests trap-assisted tunneling as the dominant transport mechanism. After annealing, a significant drop in current density indicates decrease in trap states whereas Mg-B-O device exhibits a relatively higher current density in Figure 5-4(b) resulting from the change in conduction band offset compared to MgO [8].

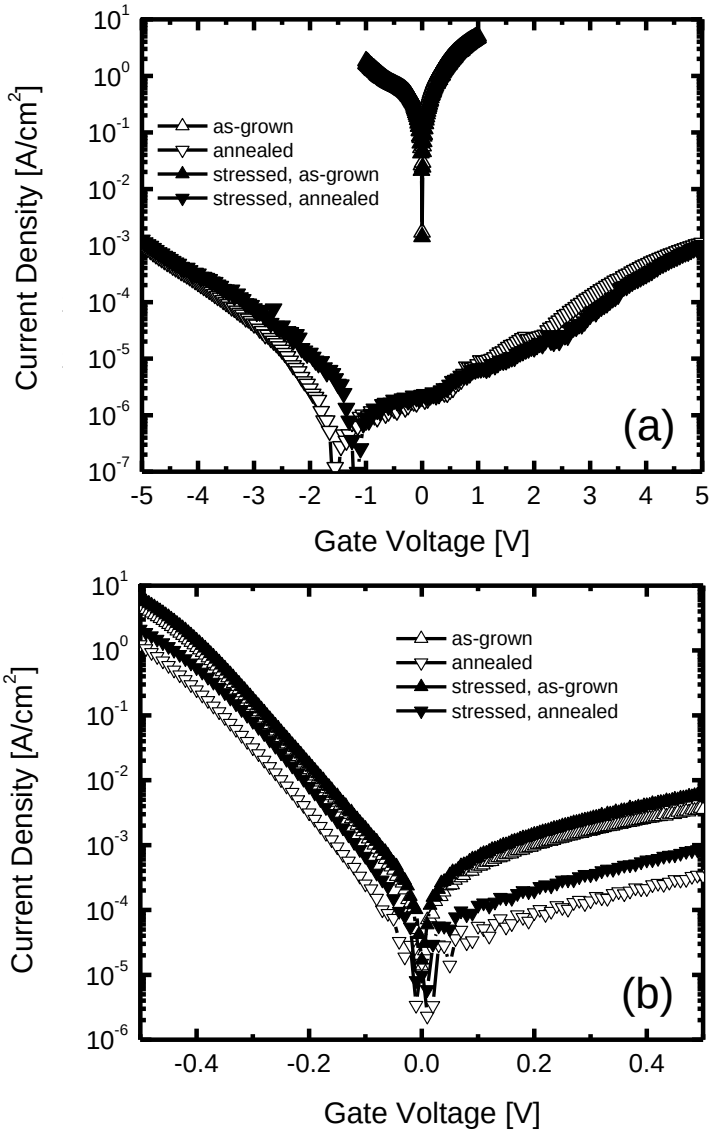



Figure 5-4 *J-V* characteristics of as-grown and annealed (a) S1 and (b) S2 devices after $10^4$ C/cm$^2$ of charges were passed through the barrier.

Figure 5-5 shows $\Delta V_{FB}$ as a function of fluence for as-grown and annealed S1 and S2. $\Delta V_{FB}$ is extracted from HFCV sweeps after stressing. If the sign of $\Delta V_{FB}$ is the same as the stress voltage (counter-clockwise hysteresis loop), substrate carrier

injection dominates. Likewise, gate injection dominates if the sign of $\Delta V_{FB}$ is the opposite of the stress voltage (clockwise hysteresis loop). For as-grown S1, the negative $\Delta V_{FB}$ after positive voltage stress ($V_s$) indicates electron injection from the gate. As discussed earlier, as-grown S1 exhibits large interfacial traps at the Ta/MgO interface, leading to carrier injection from the gate. After annealing, a smoother Ta/MgO interface is formed. Therefore, the negative $\Delta V_{FB}$ observed for as-grown S1 is likely the result of electron injection assisted by defect states located near the Ta/MgO interface. Positive $\Delta V_{FB}$ after positive voltage stress is observed under high fluence, indicating electron injection from the substrate due to trap generation near the substrate. In comparison, S2 shows negligible $\Delta V_{FB}$ under the same stress conditions before or after annealing.

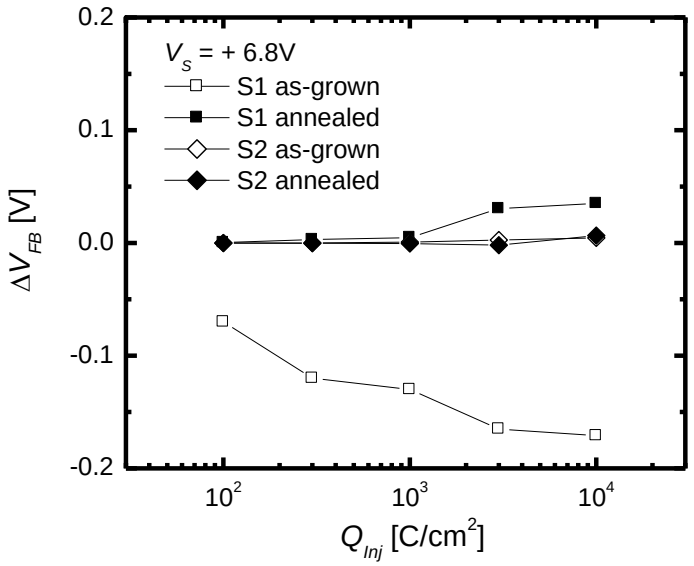



Figure 5-5 $\Delta V_{FB}$ versus the amount of electrons injected through the MTJ. $V_S$ is the stress voltage.

Figure 5-6 shows the SILC as a function of stress fluence. $\Delta J$ is the difference in current density before ($J_0$) and after stress, where a positive $\Delta J$ indicates a negative $\Delta V_{FB}$. The observed trend agrees with the results in Figure 5-5. Consistent with our previous speculation, as-grown devices are prone to SILC due to residual interface stress from sputter deposition, and the lattice mismatch at the Ta/MgO interface likely results in current-induced percolation paths, suggesting Mg-B-O to be favorable for yielding low-SILC tunnel junctions.

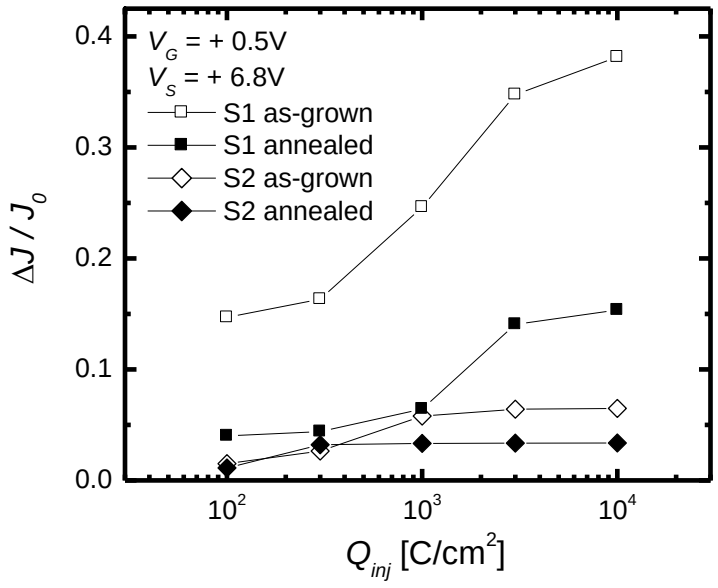



Figure 5-6 SILC as a function of injected charge, $Q_{inj}$. $V_S$ and $V_G$ are the stress voltage and sensing voltage, respectively.

Figure 5-7 and Figure 5-8 examine the amount of gate voltage shift ($\Delta V_G$) under constant current stress (CCS) of S2. For a two terminal device, negative $\Delta V_G$ signifies an increase in SILC. Consistent with previous observations, gate leakage is suppressed after annealing due to the formation of Mg-B-O and a sharper

CoFeB/MgO interface. In Fig. 5-8, it is interesting to note the transition from positive to negative $\Delta V_G$ with an increase in stress fluence from 4 to 40 C/cm$^2$. Usually, interfacial traps are generated at low stress conditions and the trapped electrons repel further injection. As we increase the fluence further, more dielectric defect sites are generated within the oxide, which increases the number of gate leakage paths and hence an increase in current. The change in current density allows us to monitor the influence of types of trap sites under different stress conditions.

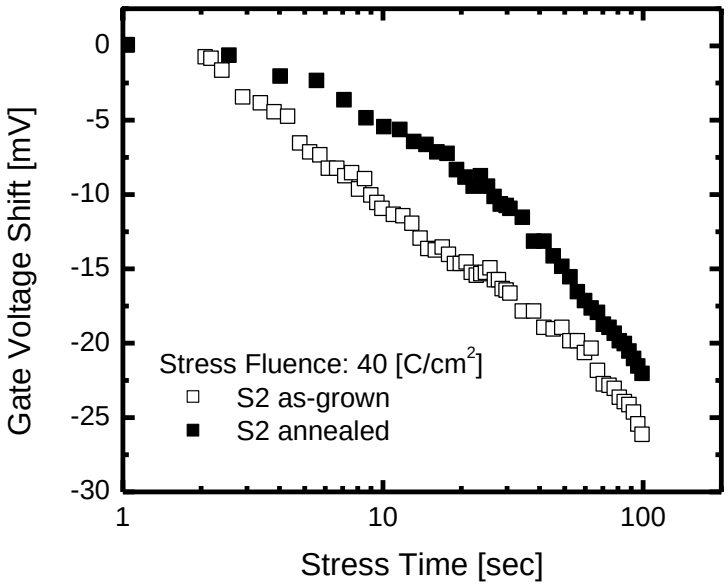



Figure 5-7 $\Delta V_G$ under constant stress fluence of 40 (C/cm$^2$) for as-grown and annealed S2.

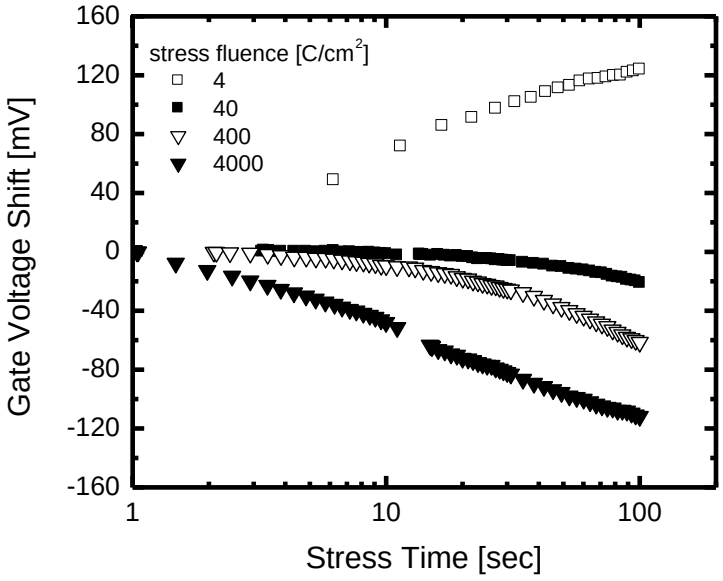



Figure 5-8 $\Delta V_G$ versus stress time under various stress fluences for as-grown S2.

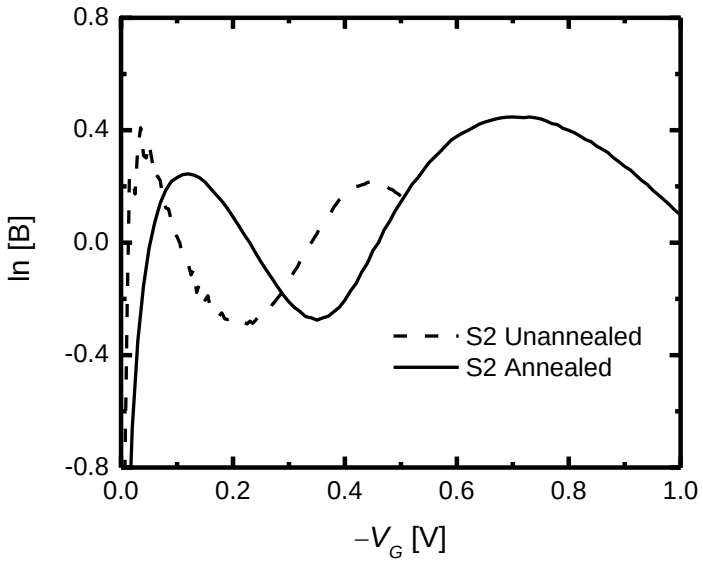



Figure 5-9 Current oscillation component as a function of $-V_G$ for as-grown and annealed S2.

Figure 5-9 shows the current quantum-oscillation component versus $-V_G$ for S2. No oscillating pattern was observed for S1. Current saturation was not observed for S1 up to −5 V. Because the current oscillation component was extracted at very small voltages for S2 (> −1 V), substrate resistance was not considered a limiting factor here. The oscillations arise due to the quantum interference of electrons in the MgO conduction band. Previous studies have shown that the oscillation pattern depends strongly on the interface roughness [20]. For rougher samples, the impinging electrons exhibit a larger range of wavelengths due to scattering, which results in poor coherence and decrease in oscillation amplitude. The oscillation peak shifts to the left due to higher local electric field and the period becomes shorter due to higher average electron energy [21]. Therefore, our results suggest that the dielectric interface becomes sharper after Mg-B-O formation, possibly leading to improved coherent spin transport.

## *5.5 Conclusion*

In summary, HFCV, conductance, IV, SILC and current oscillation measurements present a complementary characterization method to monitor how annealing and B diffusion into the MgO layer affects the trap density and stress endurance of the tunnel barrier. Our measurements indicate that as-grown Mg-B-O exhibits superior endurance behavior and post-annealing results in smoother interface, but trap states were not effectively passivated by Boron introduction.

### 5.5.1. Reflection

A direct defect density comparison between the as-deposited and annealed device was perplexed with the large defect states at the $Si/SiO_2$ interface (> $10^{13}$ $cm^{-2}$). We could deposit the MgO layer on a high quality thermally grown $SiO_2$ to better assess the change in oxide quality due to B diffusion and the subsequent annealing

processes. In addition, the interface between Ta/MgO and CoFeB/MgO is different. Again, this adds in another factor when we try to isolate the annealing effect. Perhaps it would be interesting to compare the annealing effect with different Boron composition ratios.

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# CHAPTER 6
# CONCLUSION

## *6.1 Summary of Major Contributions*

The major contributions of the work described in this dissertation are summarized as follows:

1. Demonstrated the importance of including 3-D electrostatics and channel percolation in metal NC memory statistical metrology studies. The BER was examined in various channel structures with parametrical variation that accounts for the number, density and size fluctuations in NCs.
2. Integrated redox-active CoP molecules in a Flash memory device structure using a solution-based self-assembly technique and demonstrated three programmable states at room temperature in a single cell. The monodispersion nature in size and energy levels may allow precise step-charging into a multibit memory while maintaining small bit error rate.
3. Demonstrated improved RTB-based carrier injection and enhanced $t_R / t_{PE}$ ratio of CoP-embedded NC memory cells with a LBL deposition method. The low-temperature solution-based LBL method may lead to fewer defect states at the dielectric interface, potentially creating large area, electrically robust molecular junctions.
4. A thorough electrical characterization on the CoFeB/Mg-B-O quality is performed to understand the correlation with the change in TMR and reliability under various annealing conditions.

## *6.2 Suggestions for Future Work*

A more sophisticated model of NC memory with full 3D electrostatics and current transport in both the gate-stack and channel directions will offer a more dynamic parametric study in scaled memory cells. For more accurate assessment of BER, quantum confinement and band splitting effects must be taken into account as the device dimensions enter the nanometer regime. To push the NC-based NV memory technology beyond sub-30nm, our studies suggested that a narrow-width channel is promising for better NC-substrate coupling from fringing field effects. However, previous demonstrations with CNT/ nanowire [1] is still far from real applications due to the little control of the growth process and contact resistance. Alternatively, a template structure [2] for precise NC placement may be necessary to achieve reasonably low BER at smaller dimensions.

As discussed previously, the energy state and energy separation of the embedded CoP molecules is difficult to predict due to possible charge transfer with the surrounding dielectric. However, various metalloporphyrins with different transition metals such as ZnP or CuP can be studied for comparison to verify the first order calculations on charging energy estimation. With a thorough understanding of the molecular energy alignment and Coulomb blockade energies, multiple layers or mixture of porphyrins may be integrated to increase the memory window or the number of programmable states in a single cell. However, optimization is required to achieve a reasonable programming efficiency with multiple layers of storage nodes. For molecular based memories, device reliability and repeatability has been a critical issue. Thus, endurance tests and retention measurements after cycling must also be addressed. Further optimizations of the LBL integration with ultra-thin molecular barrier and field-asymmetry enhancement should be further investigated to achieve

low thermal-budget process with reasonably small programming voltages and longer cycling lifetime.

The aforementioned molecular-RTB structure should be integrated on an organic substrate to study the interface quality, carrier transport mechanism, and observe possible improvement in $t_R$ / $t_{PE}$ for flexible electronics applications. We notice the charge storage properties strongly depend on the CNL of the surrounding dielectric in our hybrid molecular memory cells. To eliminate the defect states at the molecule-dielectric interface, one interesting study may be integrating a CoP molecule with multiple carboxyl groups to form covalent bonding with the TMA precursor of thermal ALD $Al_2O_3$ [3-4], possibly eliminating the interfacial states. Once the interface quality is improved, the surface coverage of CoP can be tuned by mixing with dummy molecules at various ratios to study interference effects.

The leakage current through an alkyl SAM is strongly influenced by the surface coverage density [5-6]. As illustrated previously, the repulsive force from the carboxyl groups of PHDA may have rendered a sparse coverage. To achieve high surface coverage with the LBL deposition method, two functional groups at opposite ends of the molecule must be chosen very carefully. One possible approach is to functionalize the tail group of the molecule after adsorption instead of depositing molecules with dual functional groups directly. Previous studies have used alkyl chains with a vinyl tail group, which can be converted into carboxyl groups with a short ozone exposure [7]. Then, the carboxyl groups may readily bond with the TMA precursors of thermal ALD $Al_2O_3$ to achieve large-area, electrically robust molecular junction due to high surface coverage density [3]. The same approach may be applied on molecular memories to improve the insulating properties of organic dielectrics.

Although a crude estimation of the CoP charging energy was discussed in Chap. 3, a more sophisticated model is necessary to calculate the self-capacitance of

the molecule. For an isolated CoP, the charging energy can be calculated by the DFT method, which gives an estimate of the electrochemical potentials and the HOMO-LUMO gap. However, the capacitance changes according to the properties of the surrounding dielectric, the distance from the electrodes, and possible interference effects from nearby molecules. With the MOS structure and the ability to control the inter-molecule distance, the above mentioned limitation is somewhat relieved, but the energy pinning effect remains problematic and the charge capture cross section, or the channel control factor of the molecule needs to be uniquely determined for different surrounding dielectric. Nevertheless, a physical-based model is of great scientific and engineering interest and would provide a complementary study for charging energy estimation and current transport characteristics of molecular-embedded tunnel barrier structure.

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